

JE40 HR

DIS/UMA/Muxless Schematics Document

Sandy Bridge

Intel PCH

DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

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Title			
Cover Page			
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JE40 HR Block Diagram (Discrete/UMA/co-lay)

SYSTEM DC/DC		CPU DC/DC	
APL5916KAI 48		NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC	
UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC	
UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC	
UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC	
NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA	
RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER	
BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

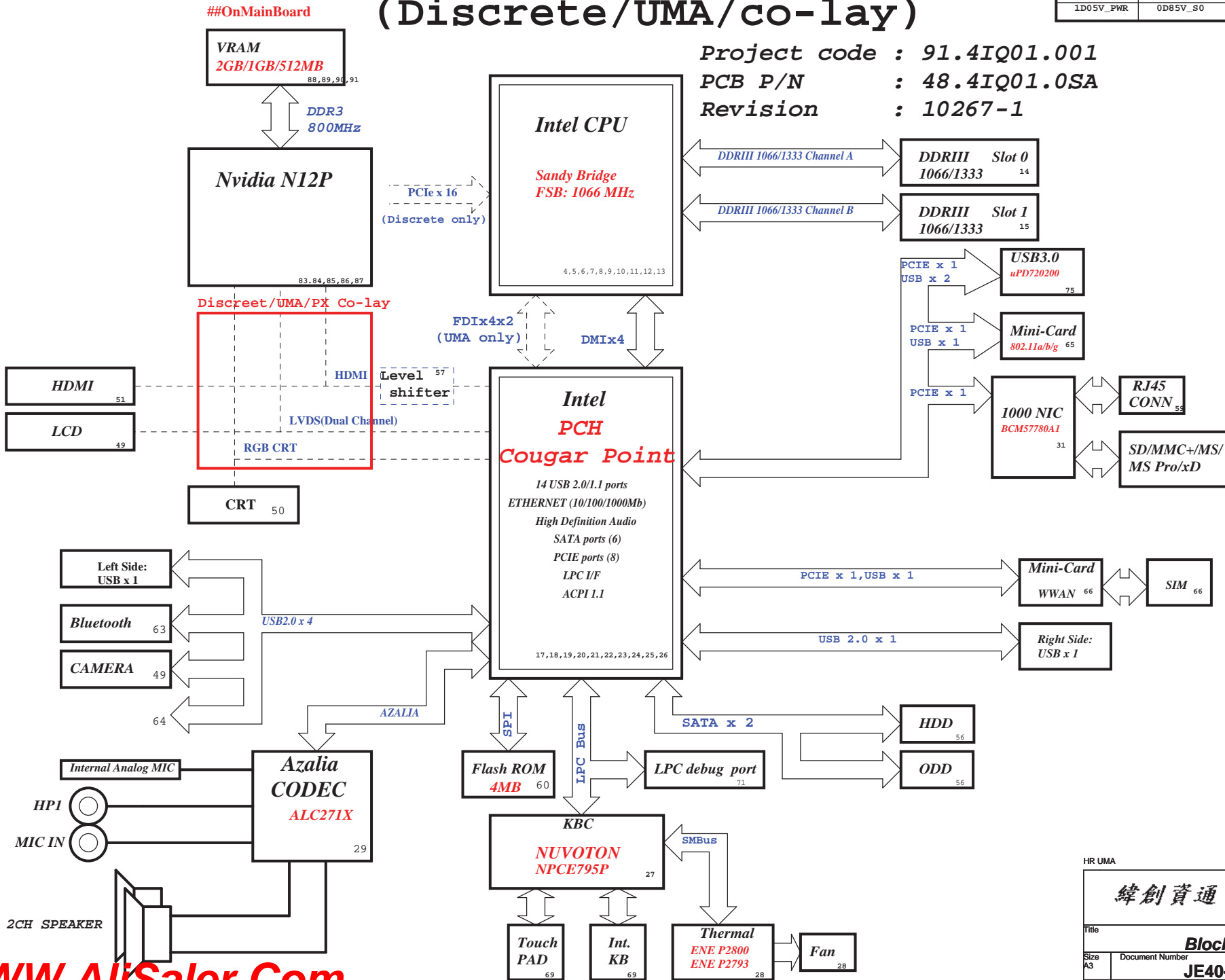
SYSTEM DC/DC	
RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC	
RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

Project code : 91.4IQ01.001
PCB P/N : 48.4IQ01.0SA
Revision : 10267-1



HR UMA

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Title			Block Diagram
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Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	


Voltage Rails			
POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCDATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

I ² C / SMBus Addresses		HURON RIVER ORB		
Device	Ref Des	Address	Hex	Bus
EC SMBus 1				BAT_SCL/BAT_SDA
Battery				BAT_SCL/BAT_SDA
CHARGER				BAT_SCL/BAT_SDA
EC SMBus 2				SMI1_CLK/SMI1_DATA
PCH				SMI1_CLK/SMI1_DATA
eDP				SMI1_CLK/SMI1_DATA
PCH SMBus				PCH_SMBDATA/PCH_SMCB
SO-DIMMA (SPD)				PCH_SMBDATA/PCH_SMCB
SO-DIMMB (SPD)				PCH_SMBDATA/PCH_SMCB
Digital Pot				PCH_SMBDATA/PCH_SMCB
G-Sensor				PCH_SMBDATA/PCH_SMCB
MINI				PCH_SMBDATA/PCH_SMCB

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Title			
Table of Content			
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SSID = CPU

CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

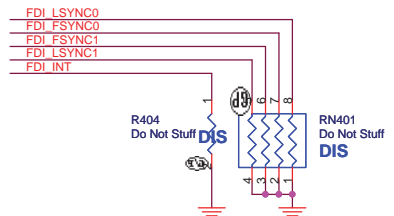
Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

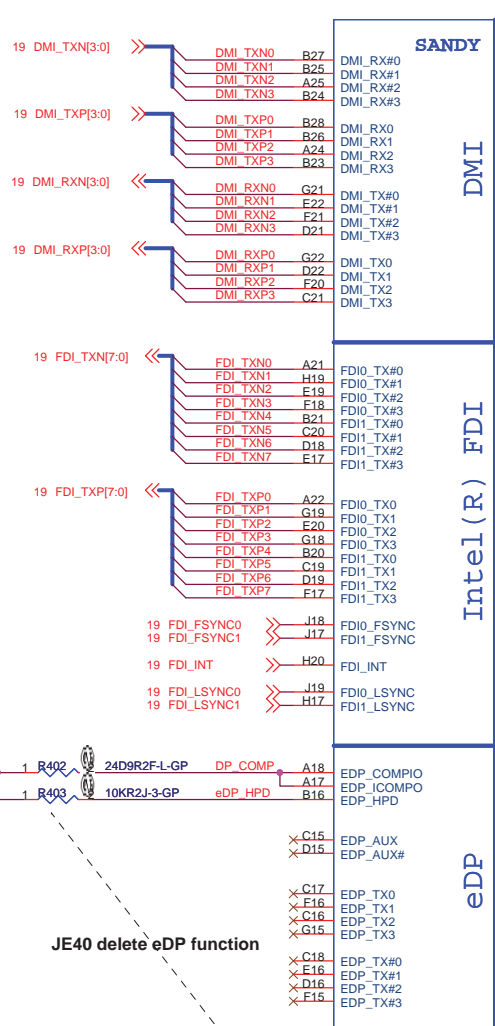
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

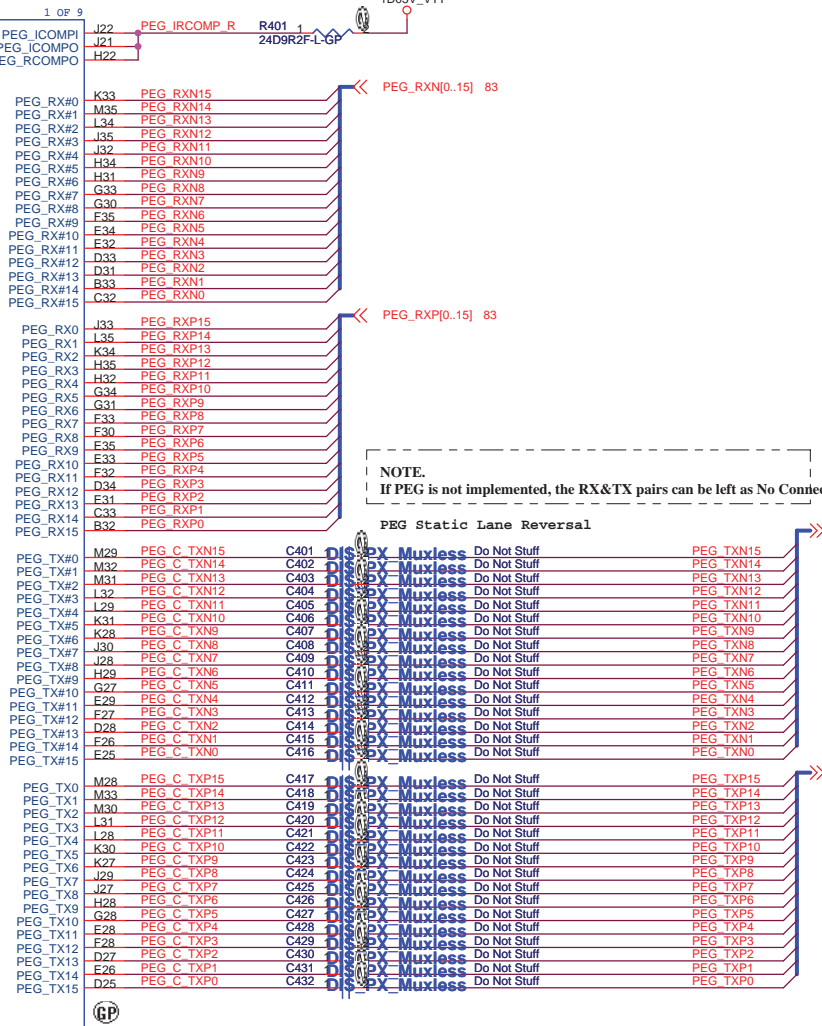
Stuff to disable internal graphics
function for power saving.



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PCI EXPRESS* - GRAPHICS



NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

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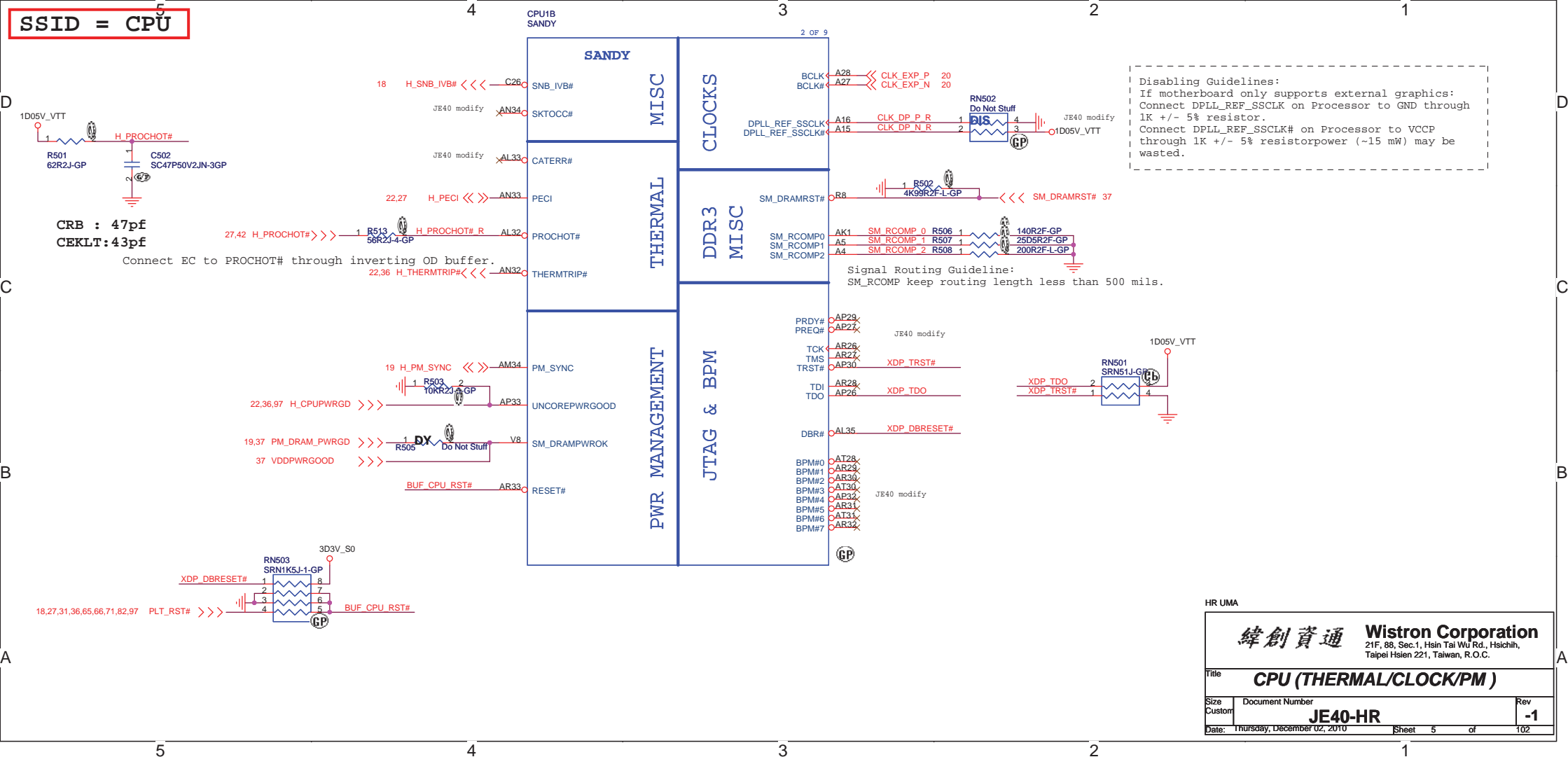
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Title
CPU (PCIe/DMI/FDI)


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SSID = CPU⁵



Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistorpower (~15 mW) may be
wasted.

Signal Routing Guideline: 
SM_RCOMP keep routing length less than 500 mils.

<div style="display: flex; justify-content: space-between; align-items: center;"> <div style="text-align: center;">  <p>緯創資通</p> </div> <div> <p>Wistron Corporation</p> <p>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</p> </div> </div>			
<p>Title CPU (THERMAL/CLOCK/PM)</p>			
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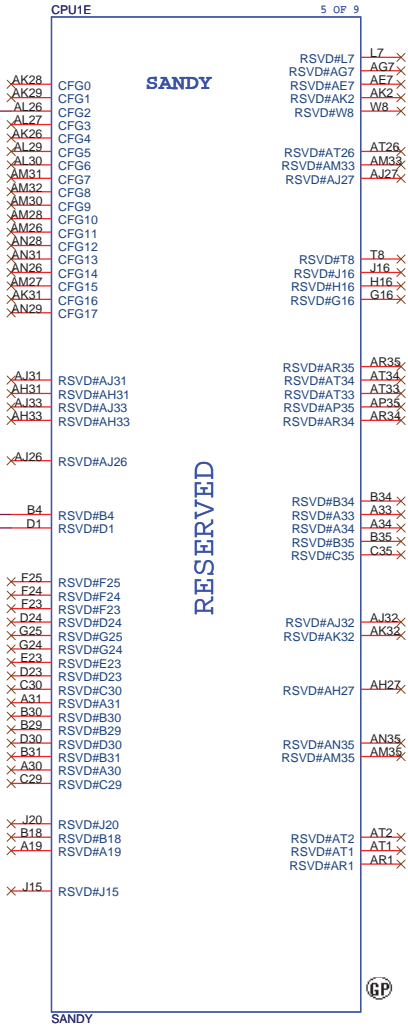
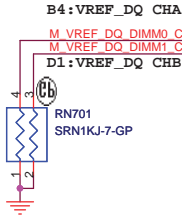
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SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

DIS_PX_Muxless

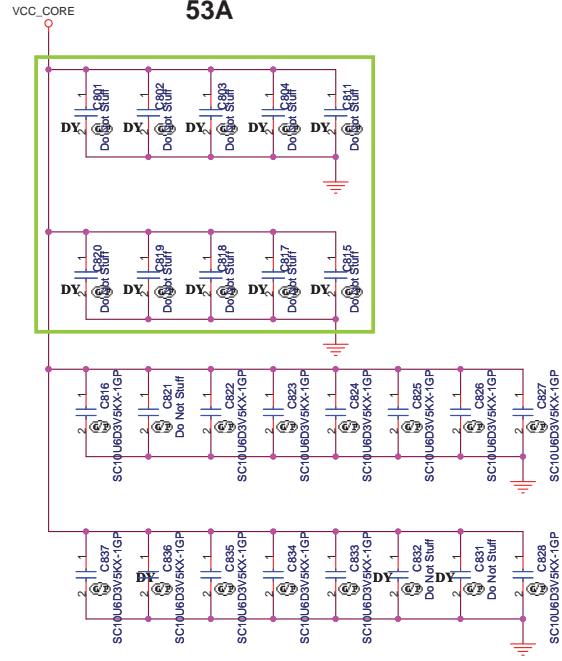


HR UMA

POWER

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

SANDY

VCC_CORE

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

PEG AND DDR

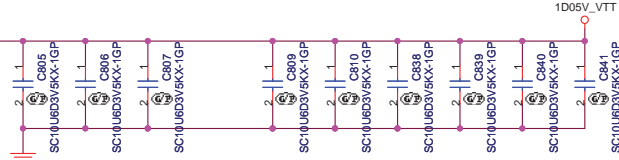
CORE SUPPLY

SVID

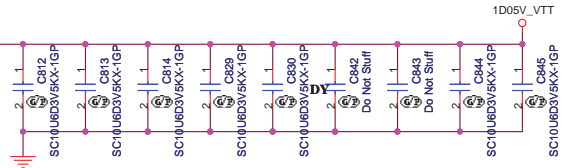
SENSE LINES

- VIDALERT#
- VIDCLK
- VIDSOUT
- VCC_SENSE
- VSS_SENSE
- VCCIO_SENSE
- VSSIO_SENSE

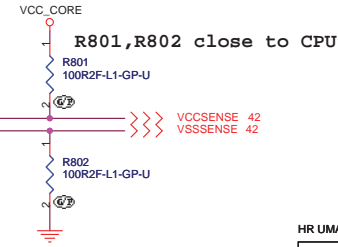
VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top



No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU



HR UMA

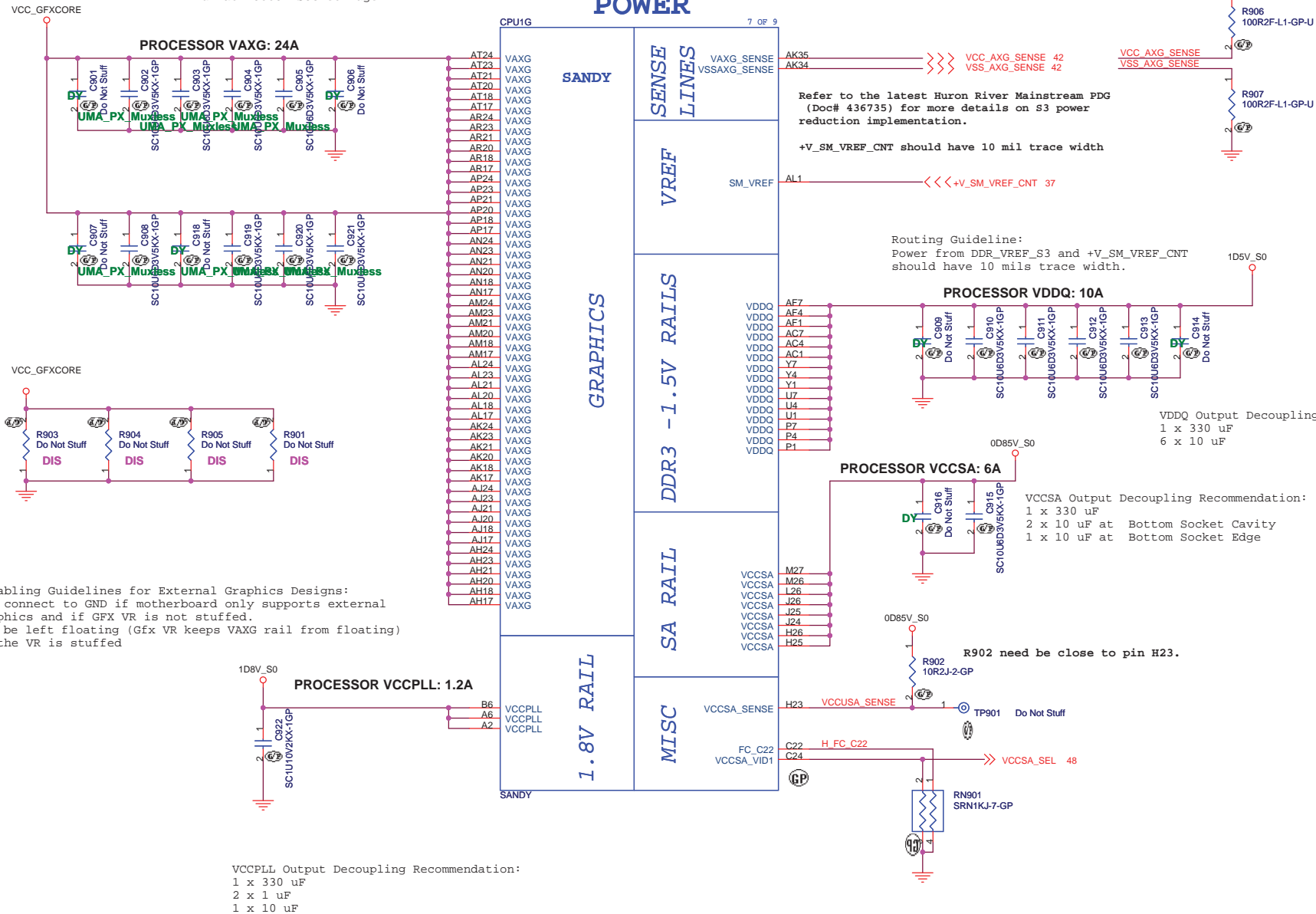
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Title CPU (VCC CORE)			
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SSID = CPU

VAXG Output Decoupling Recommendation:

- 2 x 470 uF at Bottom Socket Edge
- 2 x 22 uF at Top Socket Cavity
- 4 x 22 uF at Top Socket Edge
- 2 x 22 uF at Bottom Socket Cavity
- 4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU



Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

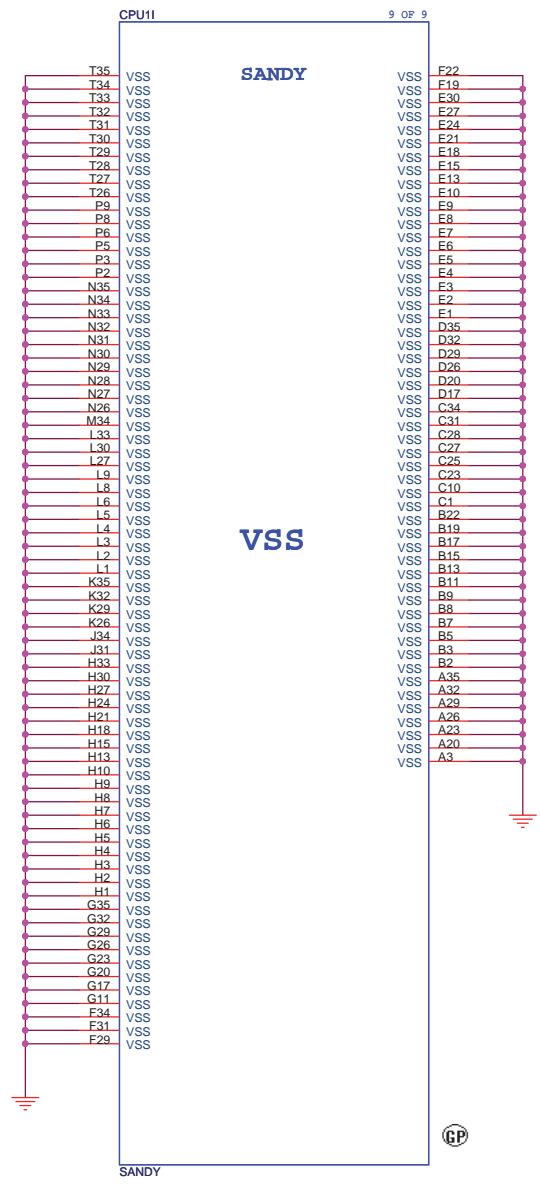
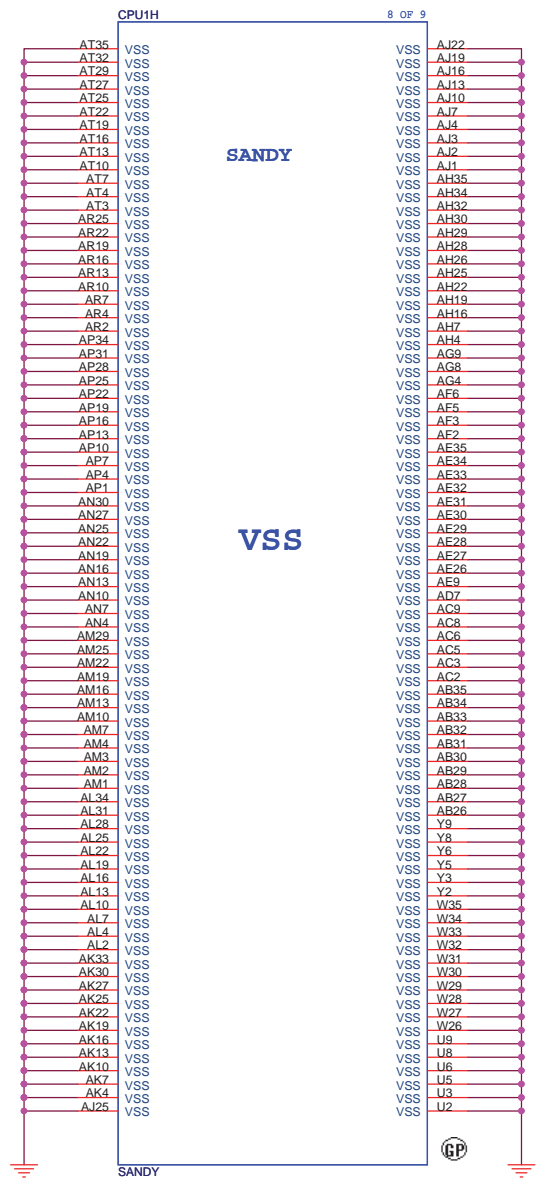
VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

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Title			
CPU (VCC GFXCORE)			
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SSID = CPU



5	4	3	2	1
D				
C				
B				
A				

JE40 delete XDP function

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<div>Title</div>			
<div>XDP</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A3</div>	<div>JE40-HR</div>		<div>-1</div>
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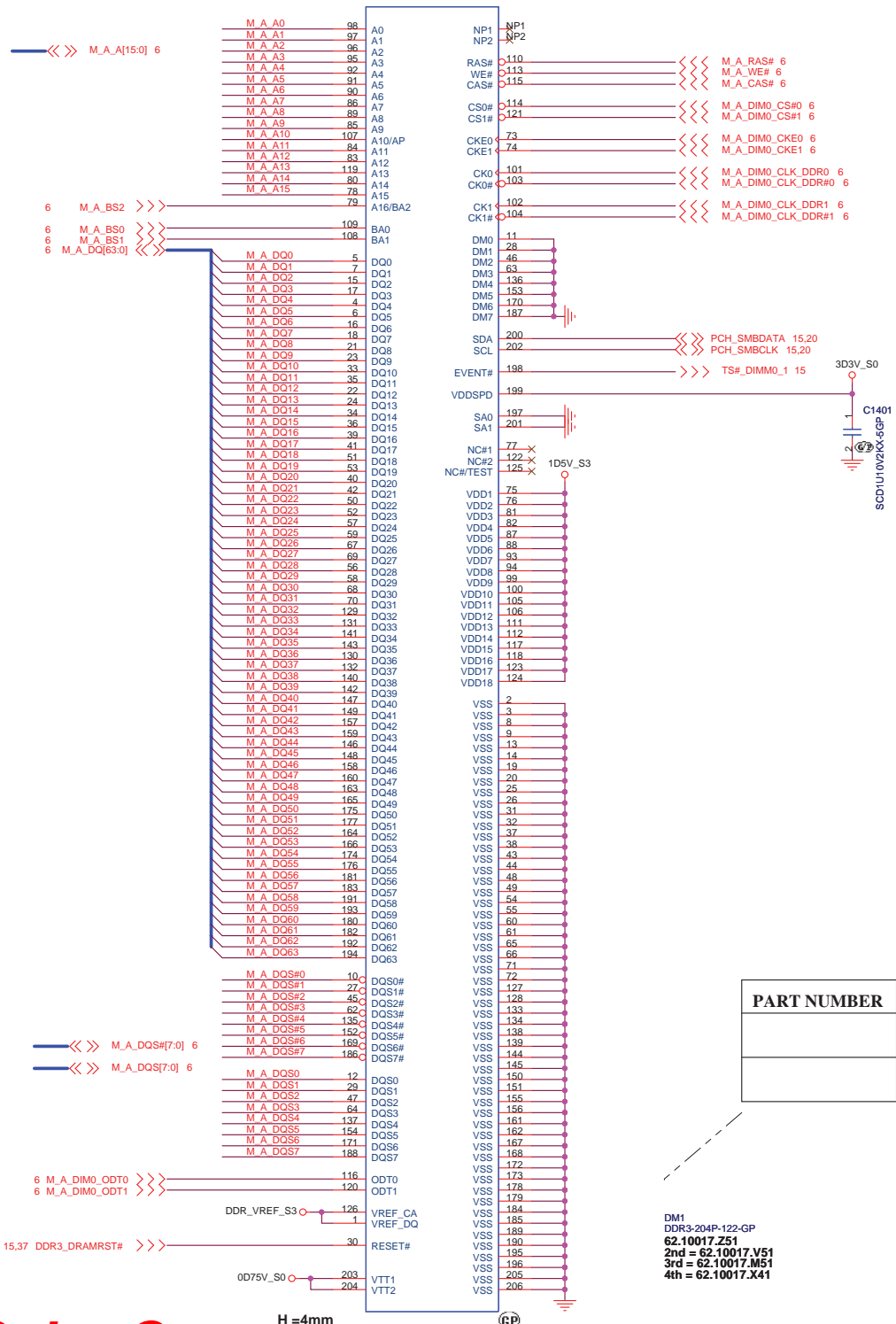
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
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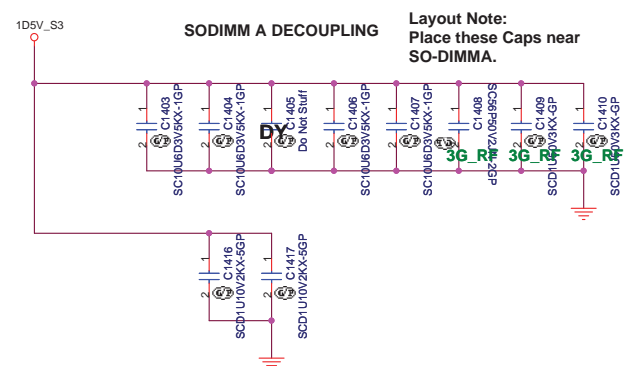
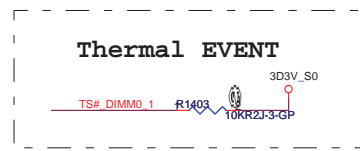
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
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SSID = MEMORY



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

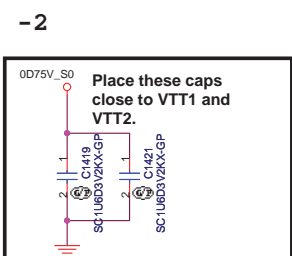
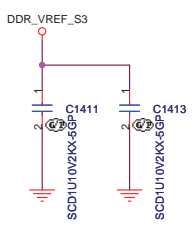
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



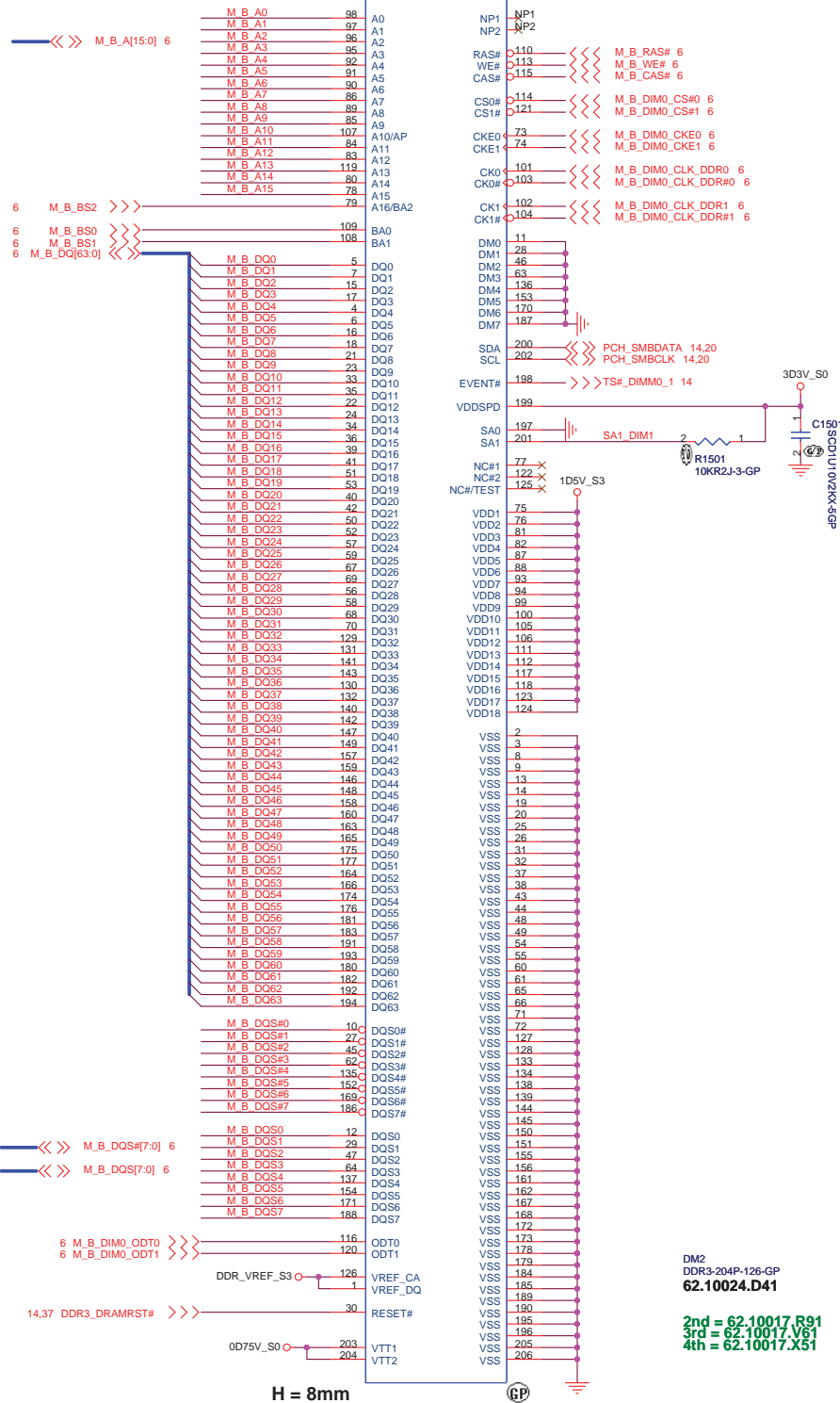
Layout Note:
Place these Caps near
SO-DIMMA.

PART NUMBER	Height	TYPE

DM1
DDR3-204P-122-GP
62.10017.251
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

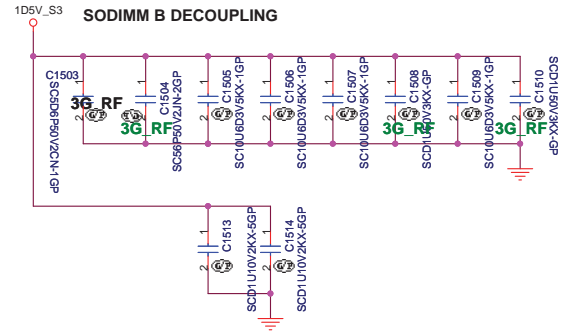


SSID = MEMORY

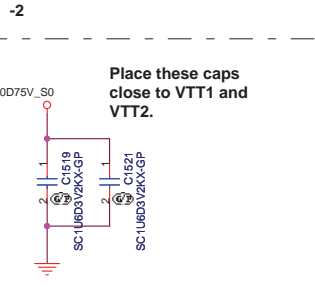
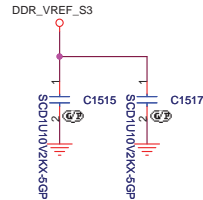


Note:
SO-DIMMB SPD Address is 0x44
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA



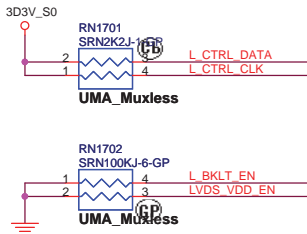
Layout Note:
Place these Caps near SO-DIMMB.



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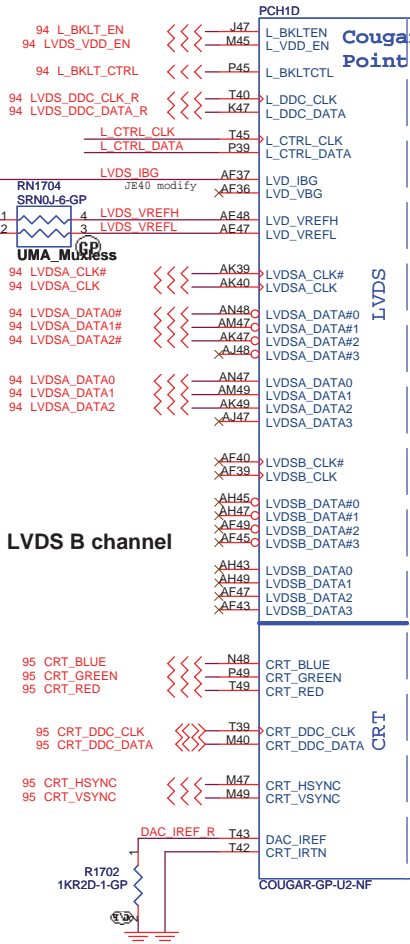
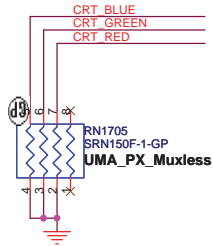
L_DDC_DATA(PAGE17):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display

Place near PCH
UMA_Muxless

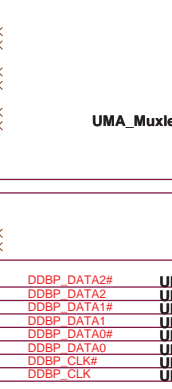
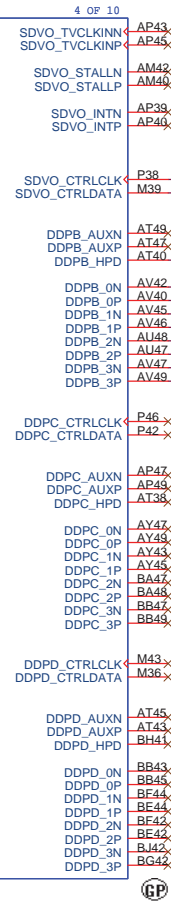
Impedance:90 ohm

JE40 delete LVDS B channel

Close to PCH side



Digital Display Interface



Close to PCH side

Impedance:90 ohm

Impedance:100 ohm

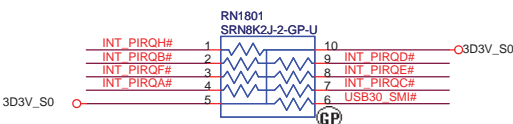
Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPDP	NA	DDPB_HPDP	HDMIIB_HPDP
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIIB_CTRLDATA

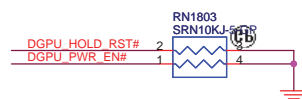
HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

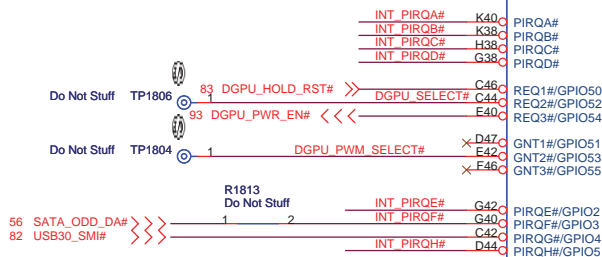
SSID = PCH



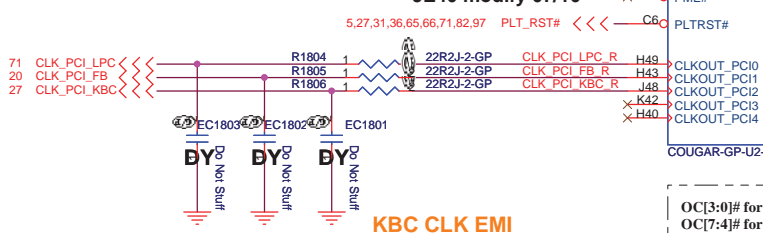
Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



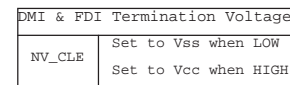
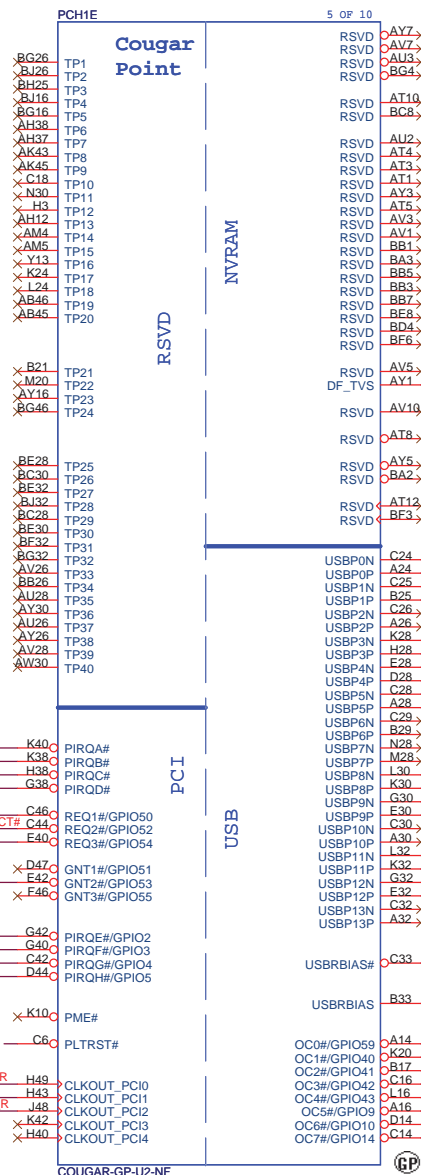
BOOT BIOS Strap		
GNT1#/GPIO51	SATA16P/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



JE40 modify 07/16



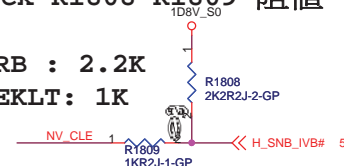
OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)



check R1808 R1809 阻值

CRB : 2.2K

CEKLT: 1K



✖ USB Ext. port 1 (HS)

```

External debug port use on Huron river platform

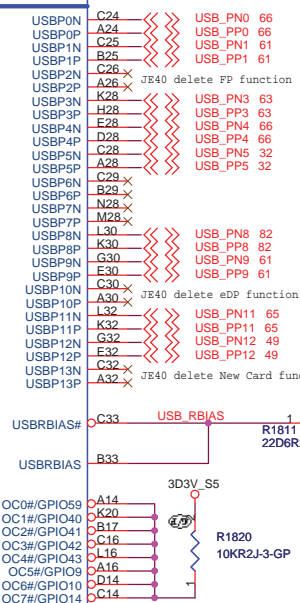
```

USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB C
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SB add USB port 5

JE40 co-lay USB2.0



USB 2.0 Overcurrent Pin Default Usage

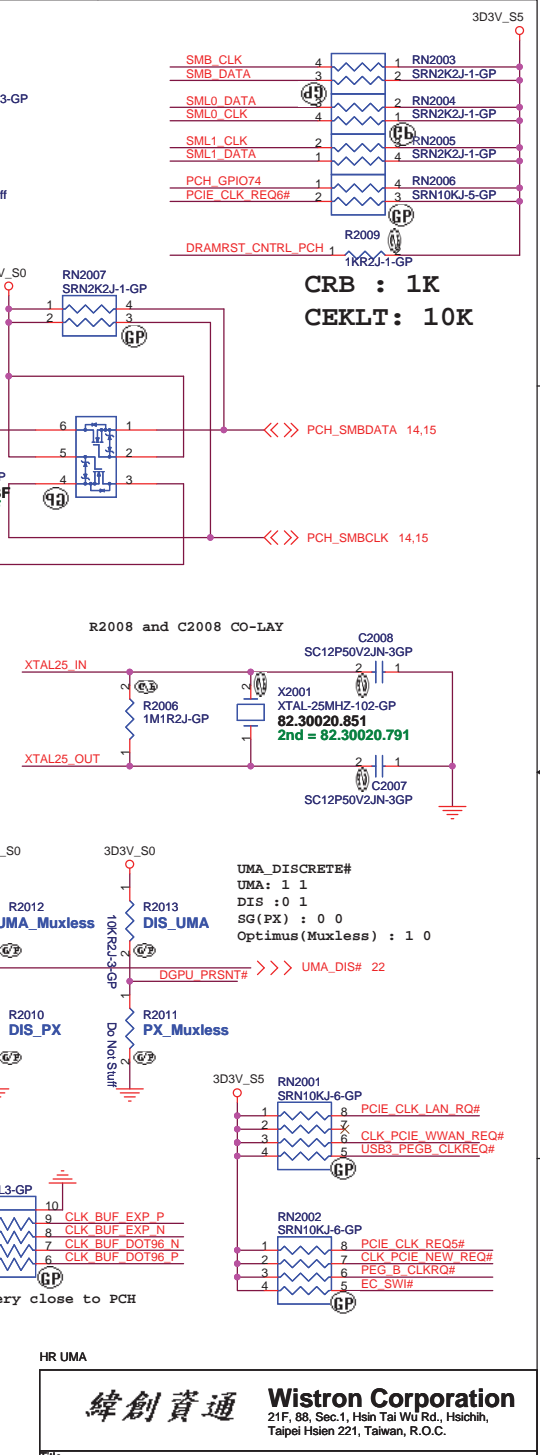
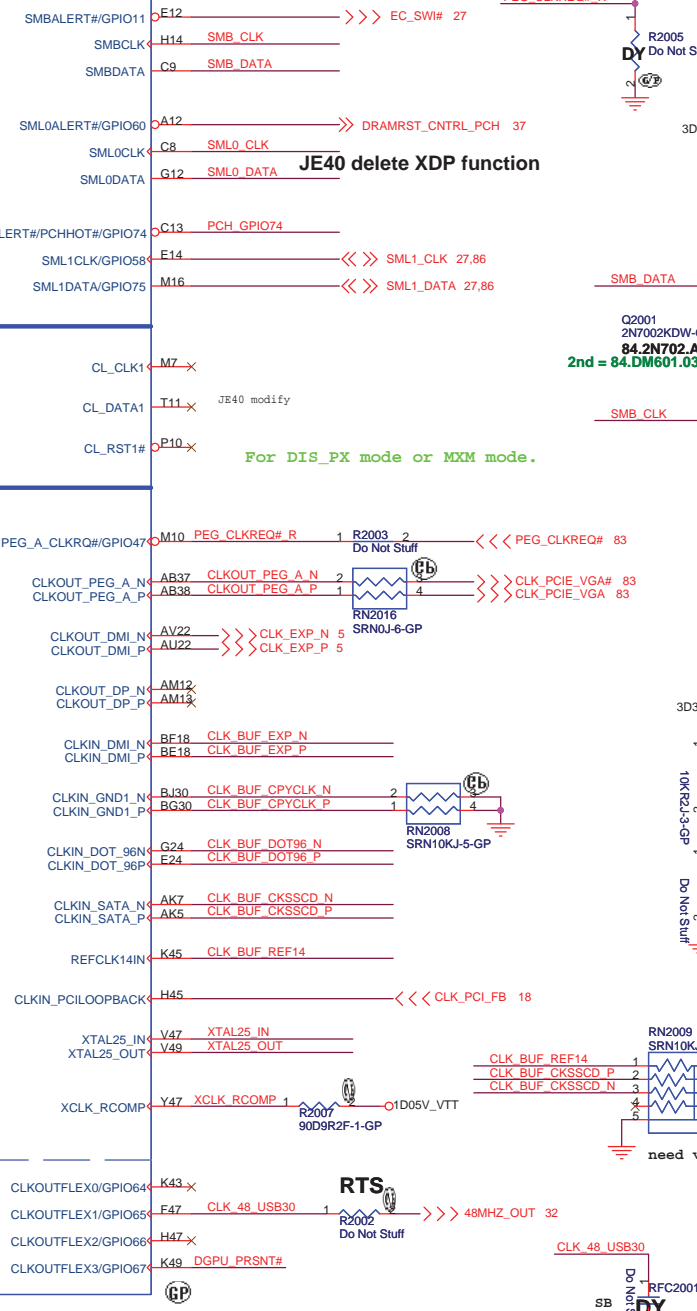
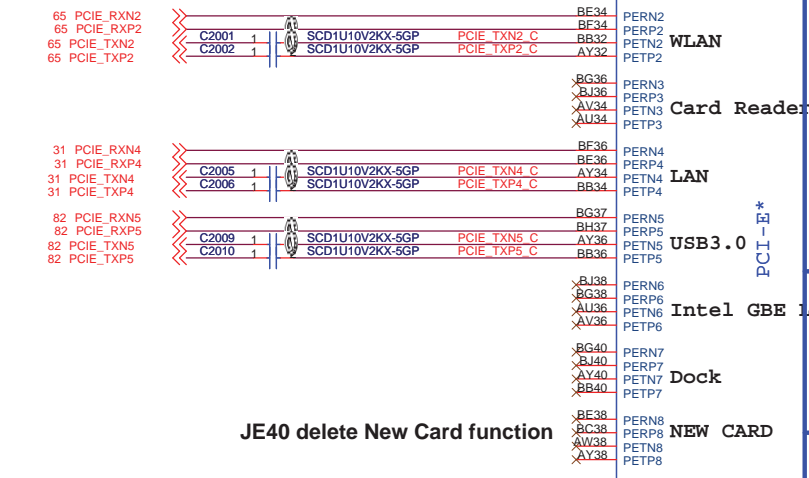
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

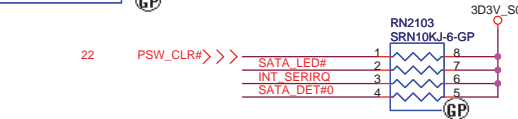
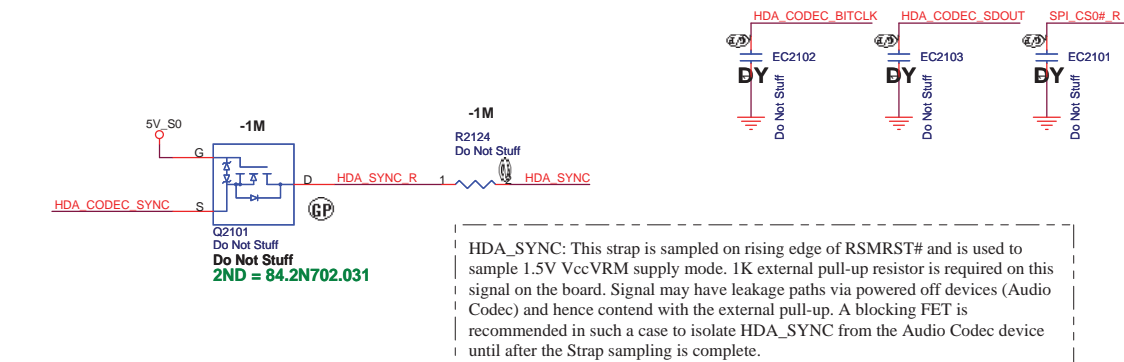
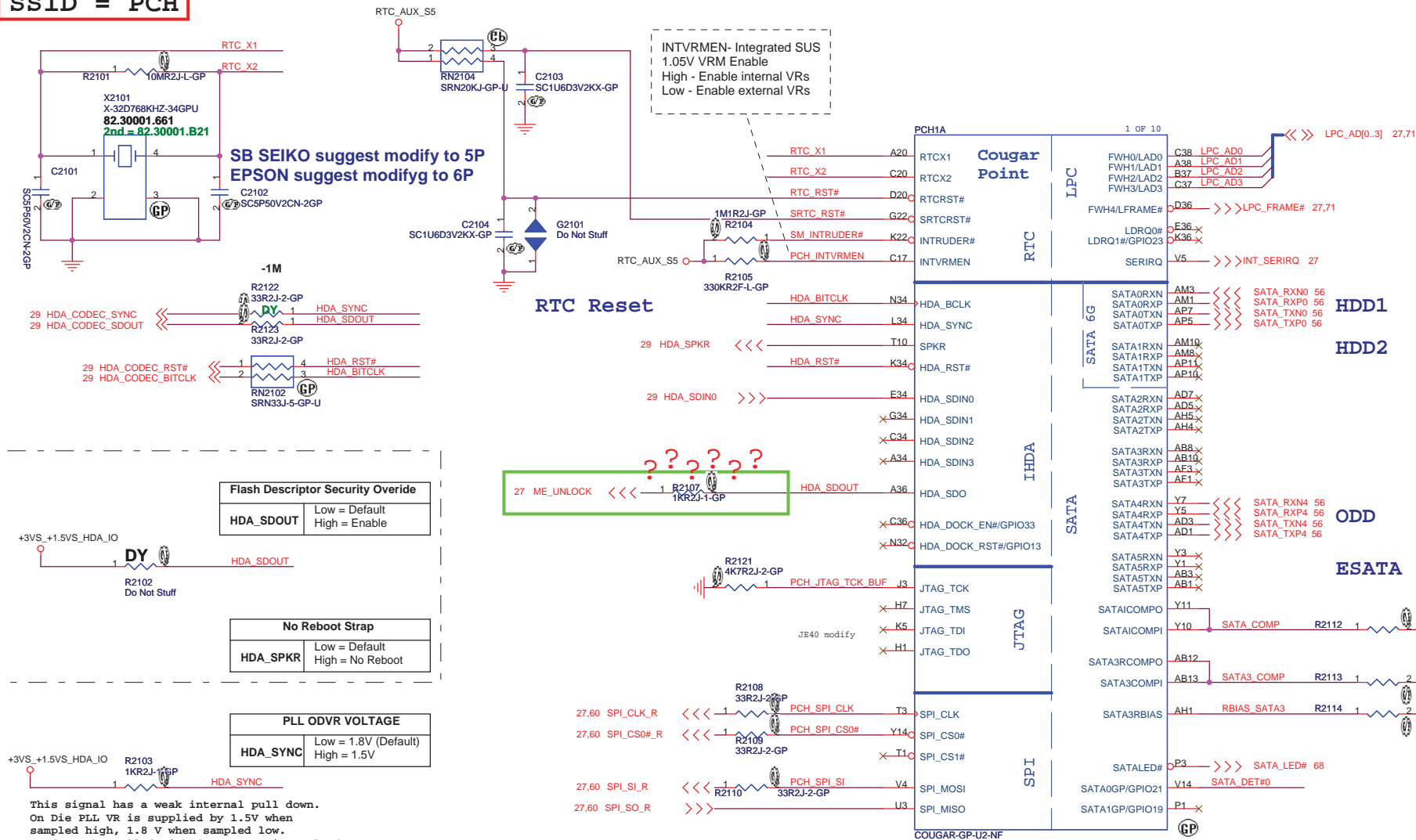
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			
PCH (PCI/USB/NVRAM)			
Size A3	Document Number		Rev
	JE40-HR		-1
Date:	Thursday, December 02, 2010		Sheet 18 of 102

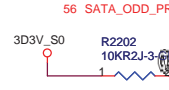
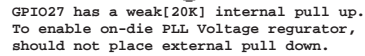
SSID = PCH



SSID = PCH



Note:
For PCH debug with XDP, need to NO STUFF R2218

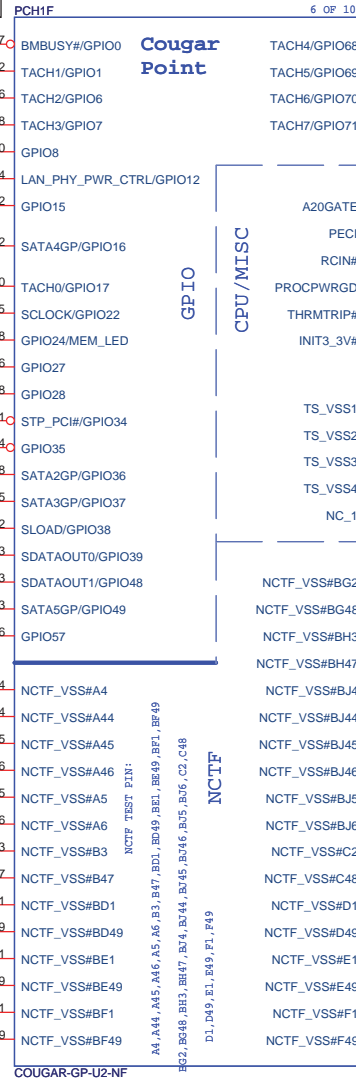
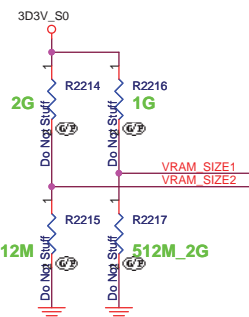
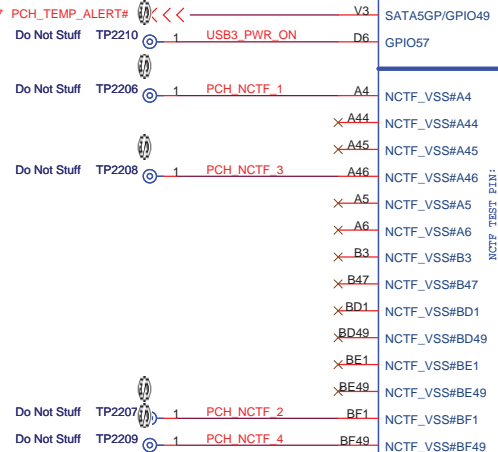
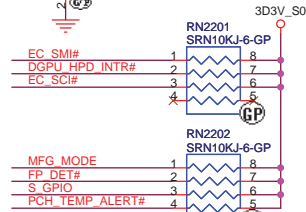


92,93 DGPU_PWROK

0806 delete TP2202, TP2203
Do Not Stuff TP2202
Do Not Stuff TP2203

21 PSW_CLR# <<<

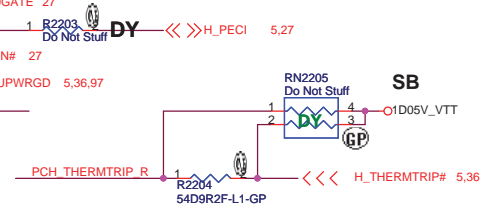
JE40 delete FP function



```

CH4/GPIO68  C40  >>> SATA_ODD_PWRGT  56
CH5/GPIO69  B41  >>> UMA_DIS#   20
CH6/GPIO70  C41  VRAM_SIZE1
CH7/GPIO71  A40  VRAM_SIZE2

```



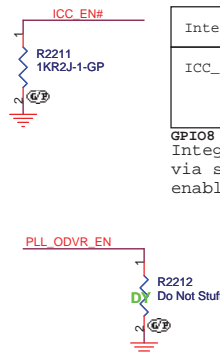
TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT] LOW (R2211)- ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.



HR UMA

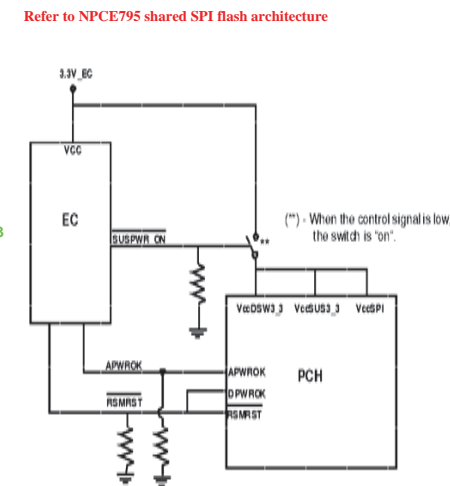
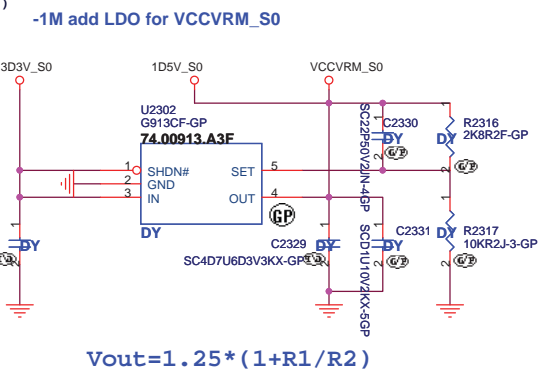
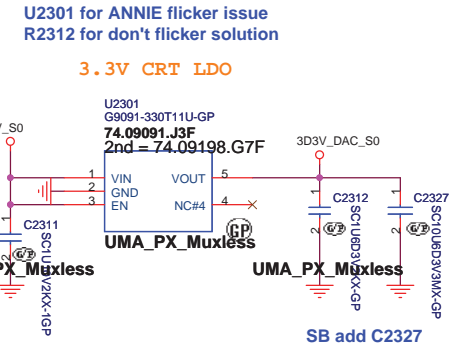
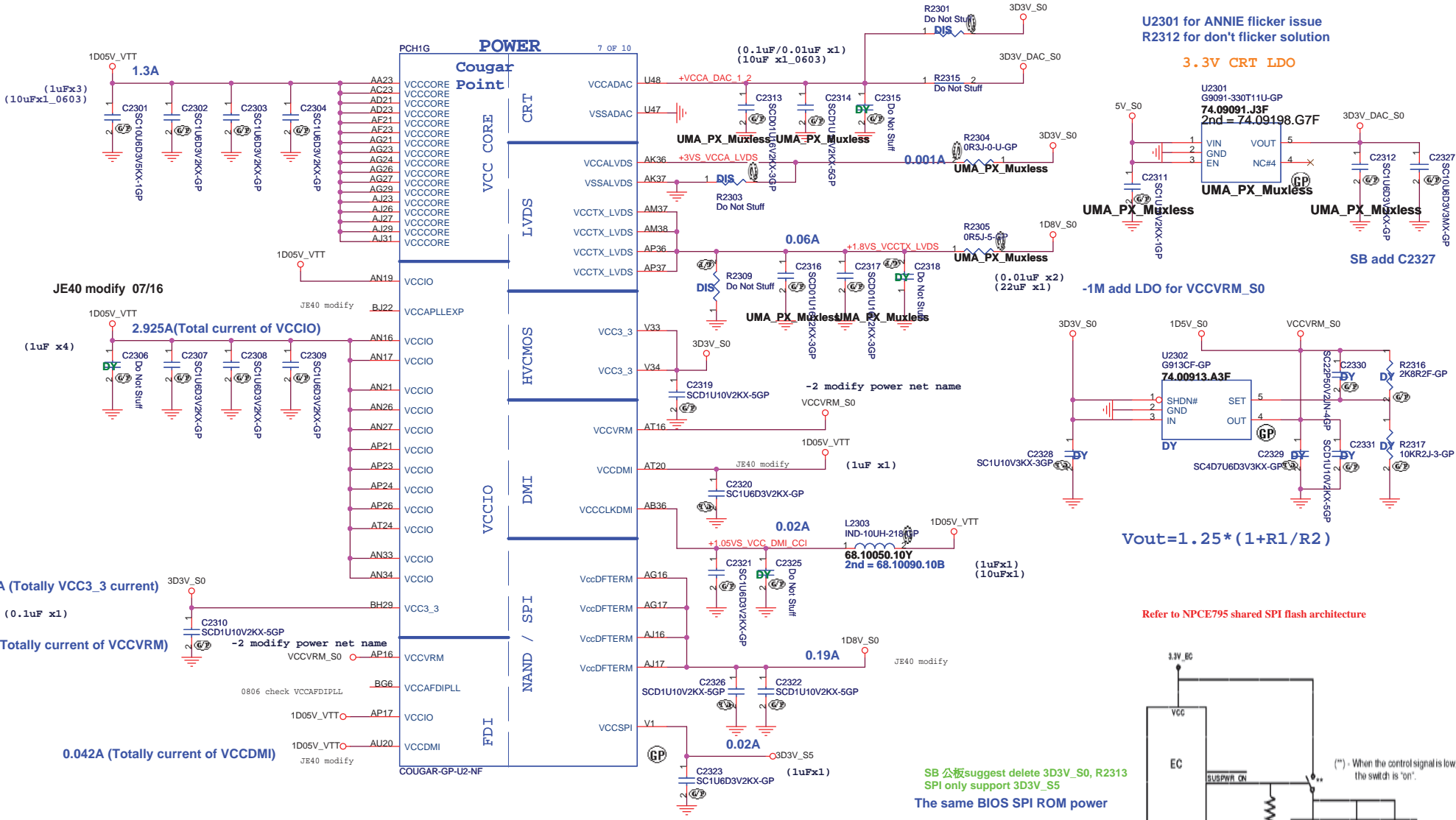
緯創資通 **Wistron Corporation**
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Title			
PCH (GPIO/CPU)			
Size A3	Document Number		Rev
	JE40-HR		-1
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PLL ON DIE VR ENABLE

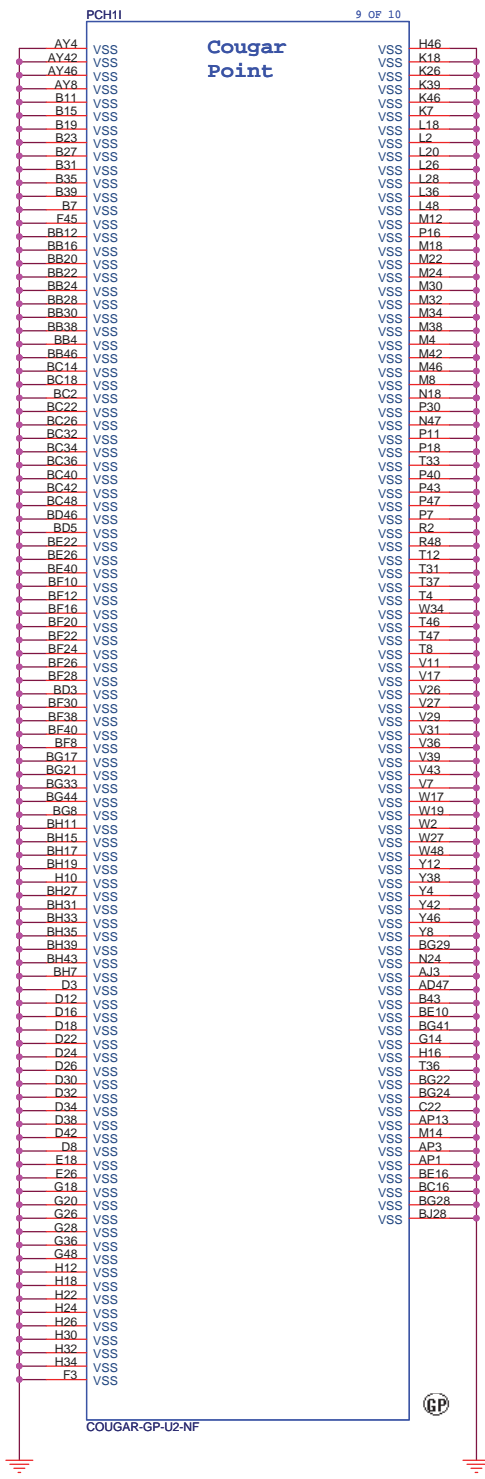
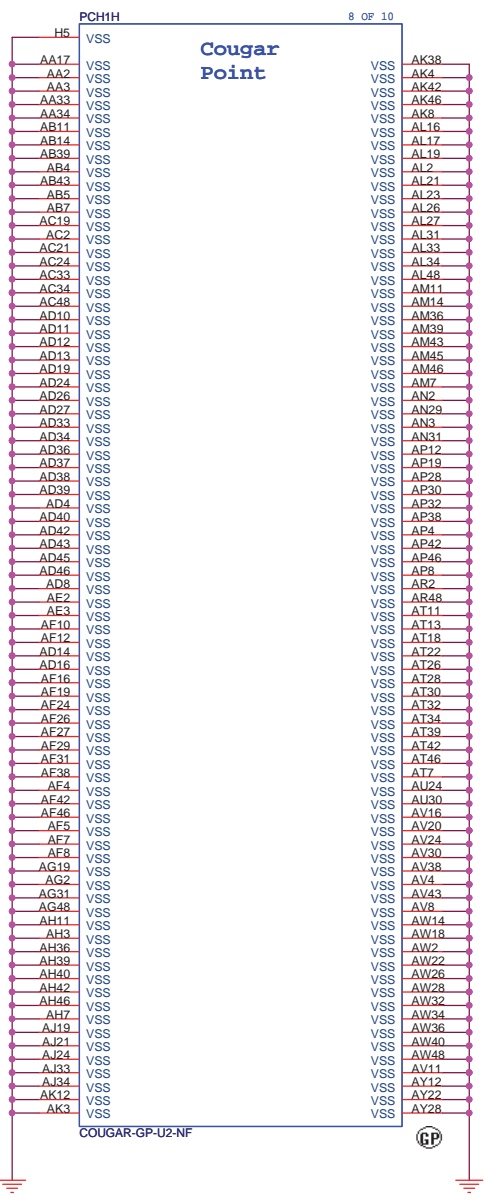
NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

WWW.AliSaler.Com



SB 公板 suggest delete 3D3V_S0, R2313
SPI only support 3D3V_S5
The same BIOS SPI ROM power

SSID = PCH



HR UMA

緯創資通 Wistron Corporation

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Title

PCH (VSS)

Size A3

Document Number

JE40-HR

Date: Thursday, December 02, 2010

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Rev -1

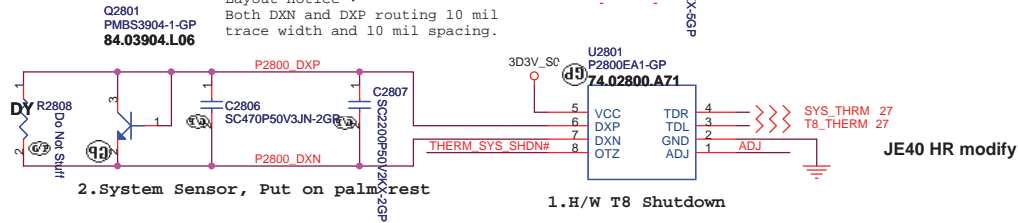
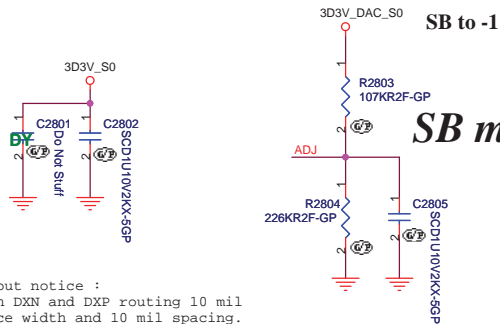
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Clock(colay)		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 26 of 102



SSID = Thermal

Thermal sensor P2800



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

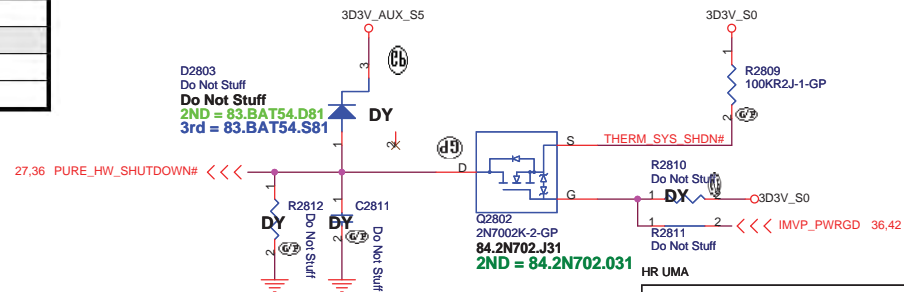
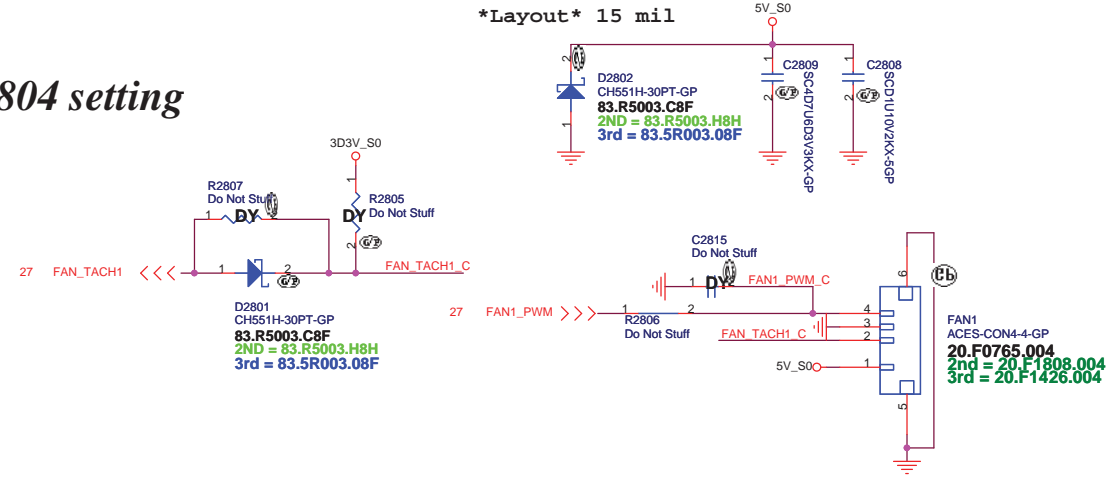
RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (V)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

VGA Thermal sensor P2800

SMBUS modify to Page 84

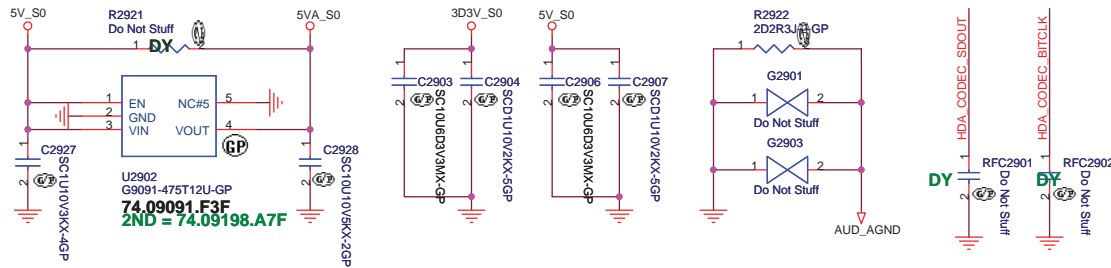
Fan controller P2793

Layout 15 mil



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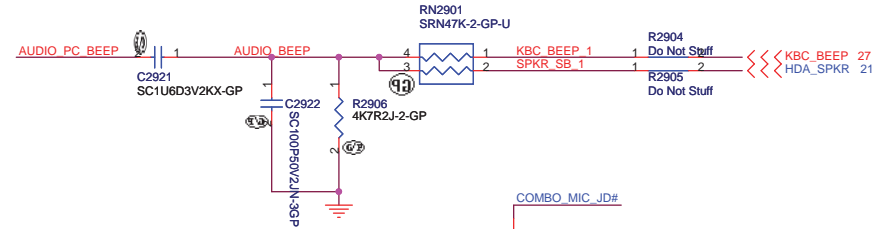
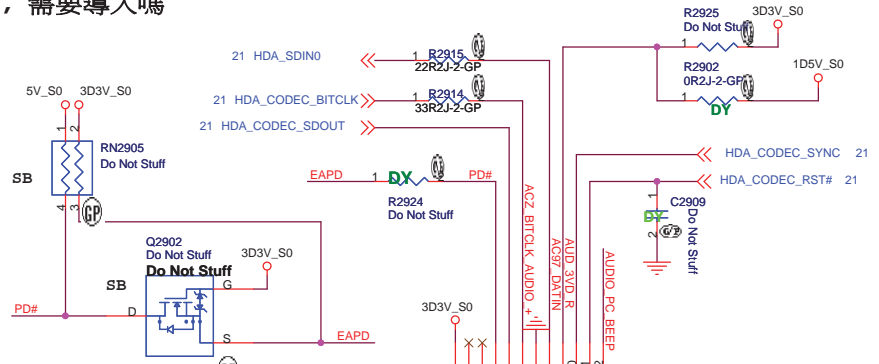
Title		Thermal P2800/Fan Controller P2793	
Size	Document Number	JE40-HR	
Custom		-1	
Date:	Thursday, December 02, 2010	Sheet	28 of 102



CLOSE TO PIN39 and 46

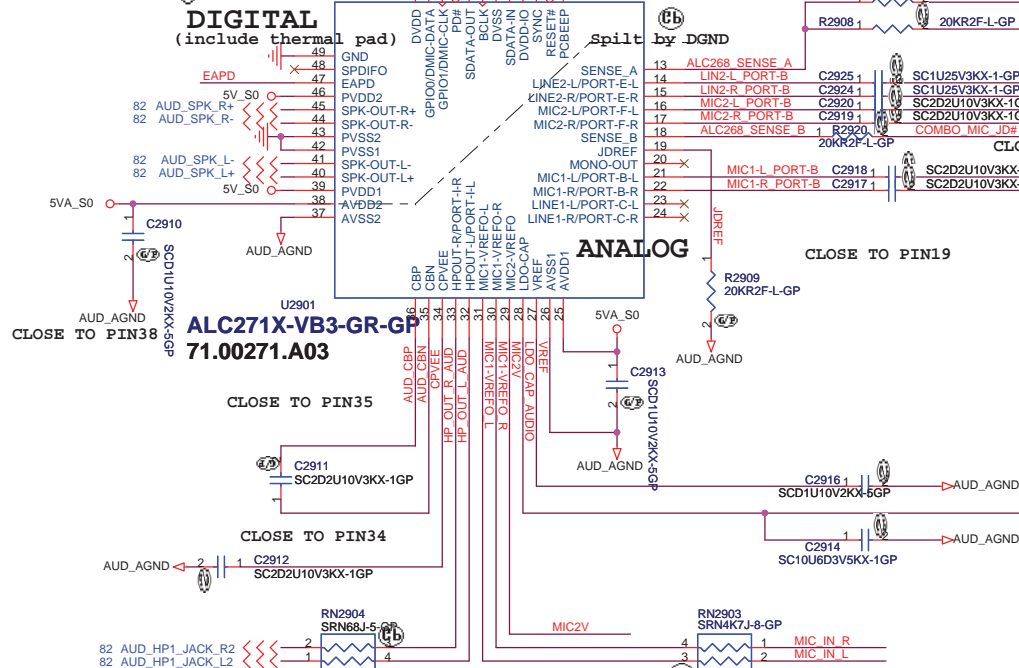
-1 PVDD timing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎

CLOSE TO PIN1 and 9



Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V

MIC2V Ref voltage is 2.5V
because Vgs(th) concern
cann't use 2N702 for desing



CLOSE TO PIN18

CLOSE TO PIN19

SB modify

HR UMA

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Audio Codec		
Size A3	Document Number	Rev
	JE40-HR	-1
Date: Thursday, December 02, 2010	Sheet 29	of 102

AUDIO OP AMPLIFIER

JE40 delete AMP function

HR UMA

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Audio AMP

Size
A4

Document Number

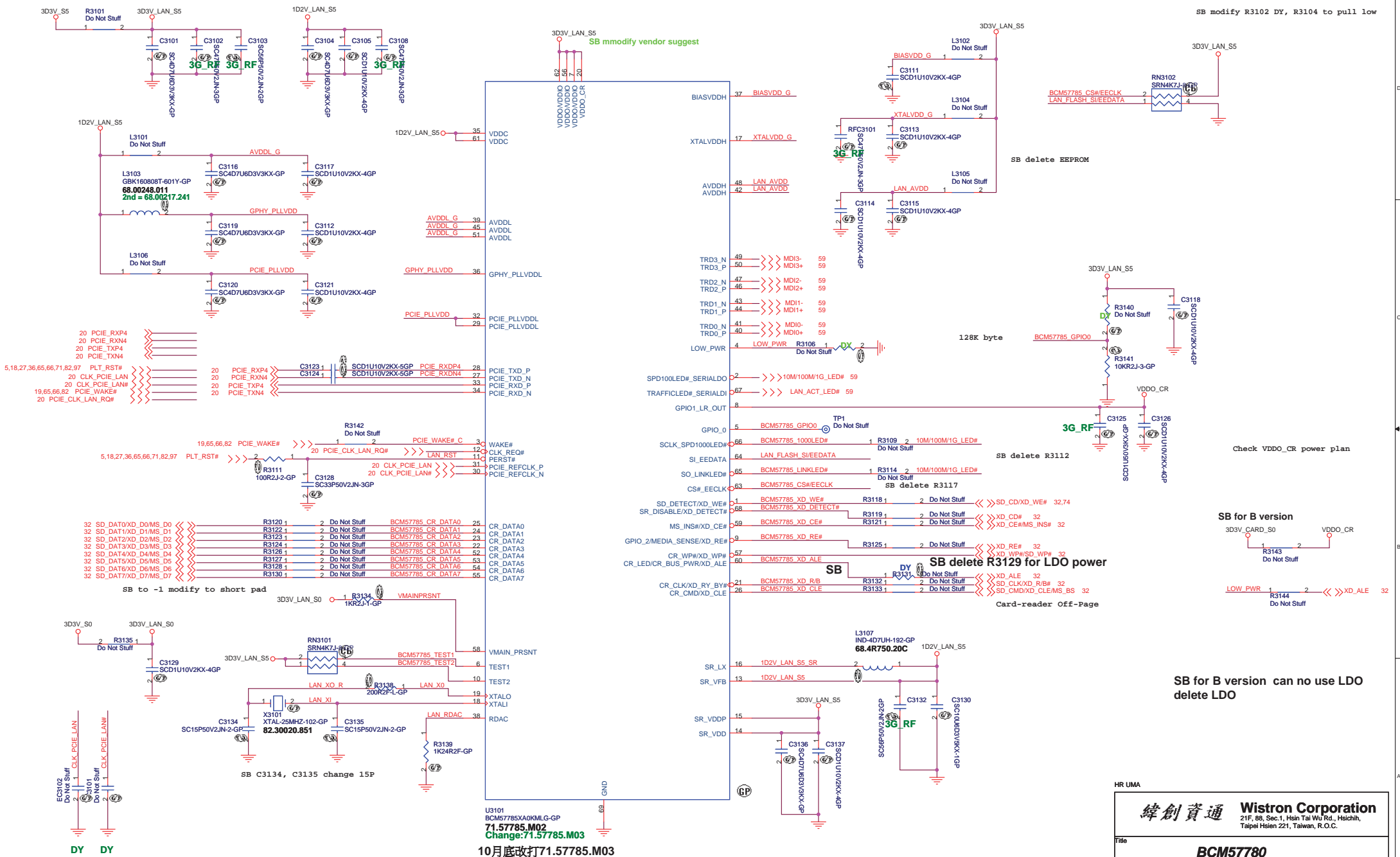
JE40-HR

Rev
-1

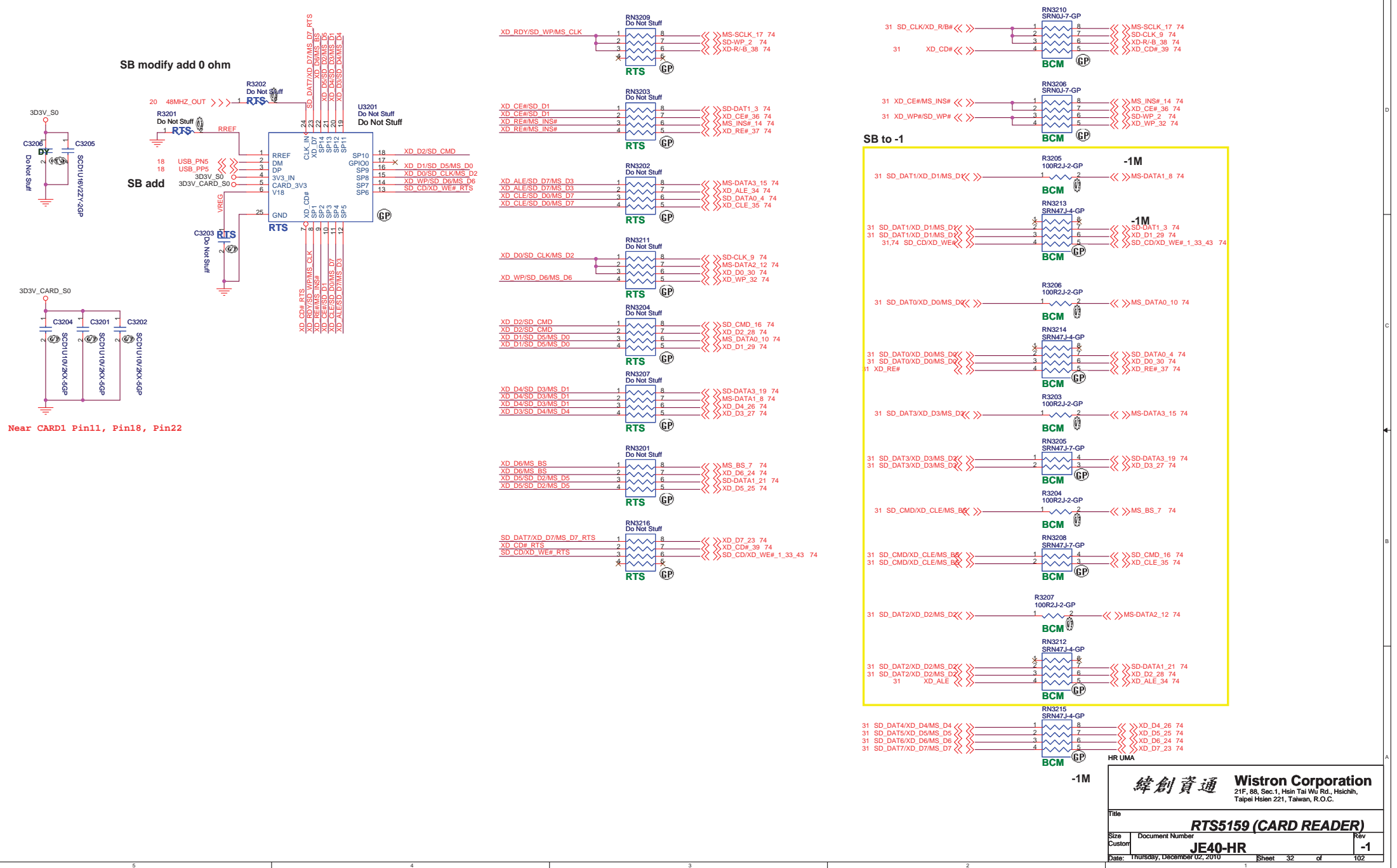
Date: Thursday, December 02, 2010

Sheet 30 of 102

SB modify L3101,2,4,5,6 to 0 ohm



HR UMA			
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Size		Rev	
Customer	Document Number	-1	
Date		Sheet	
Tuesday, December 02, 2010		31	102



(Blanking)

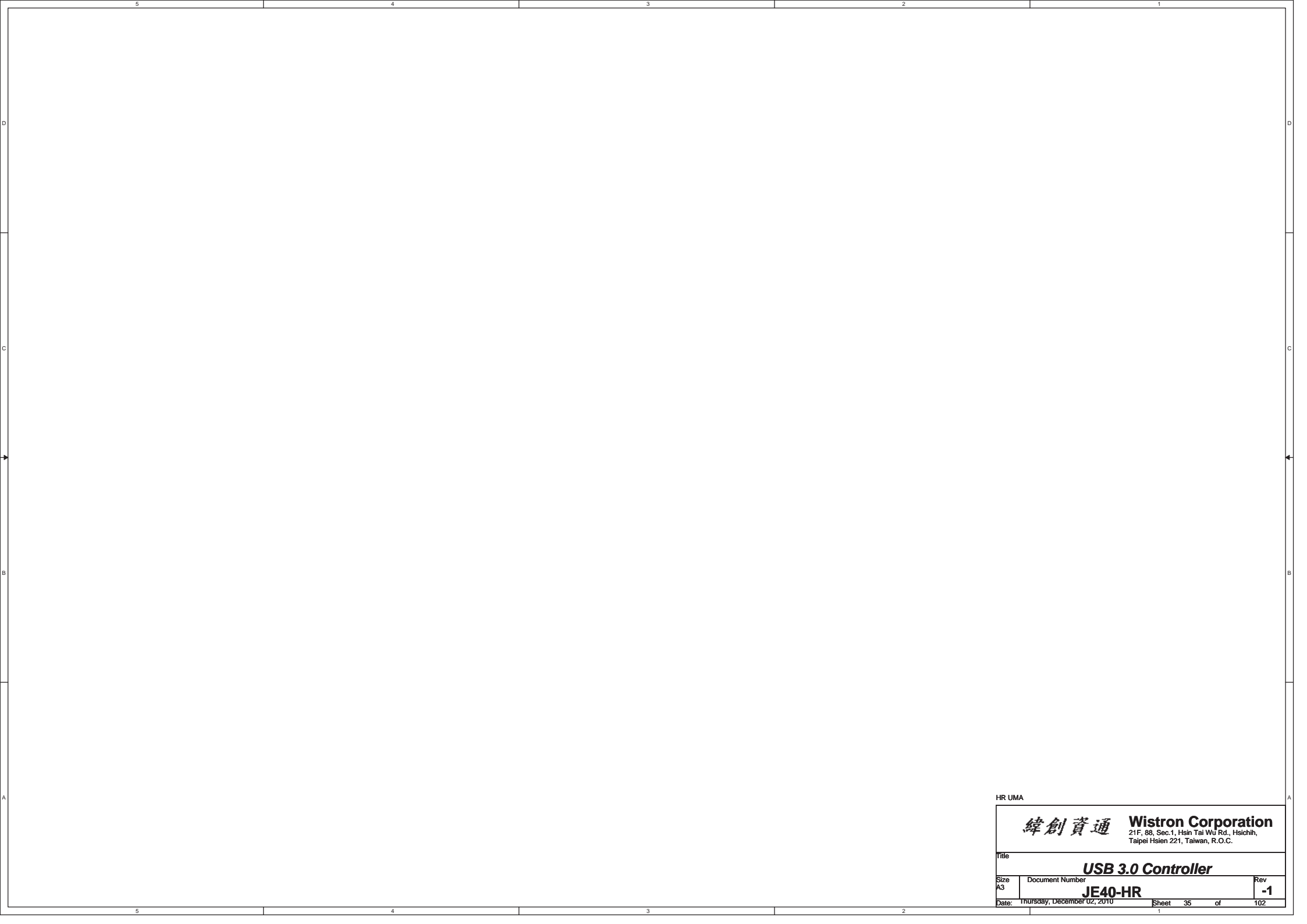
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 33 of 102

(Blanking)

HR UMA

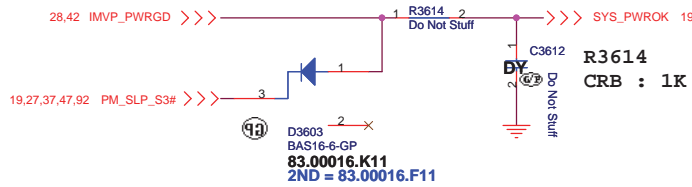
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 34 of 102



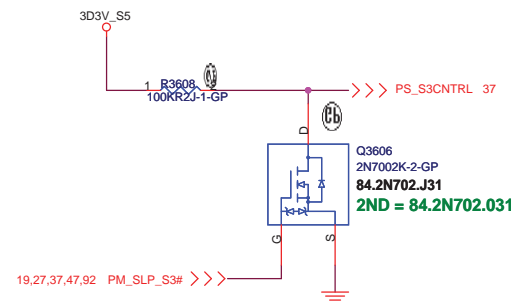
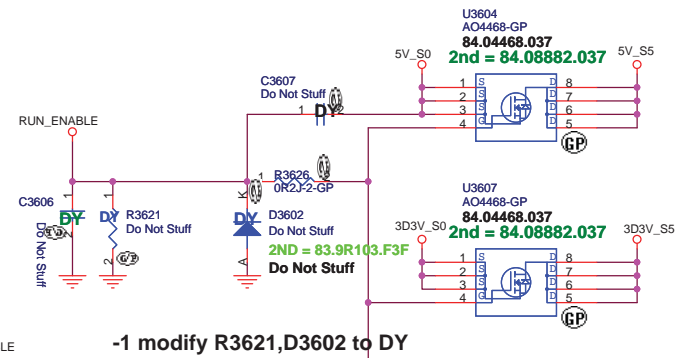
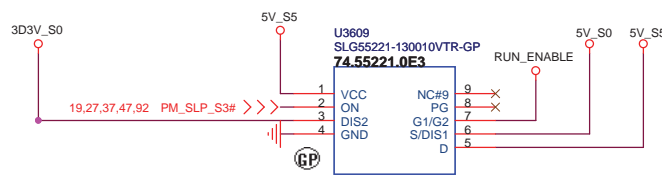
HR UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Controller			
Size A3	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010	Sheet	35 of	102

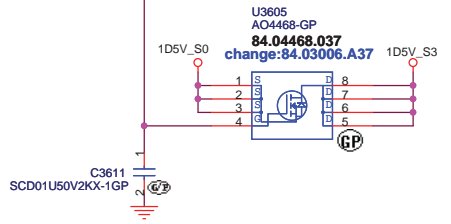
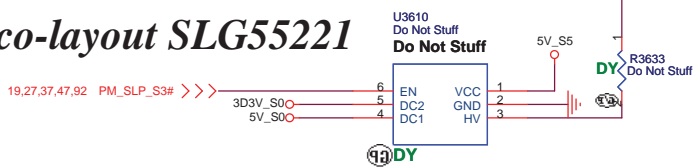
Power Sequence



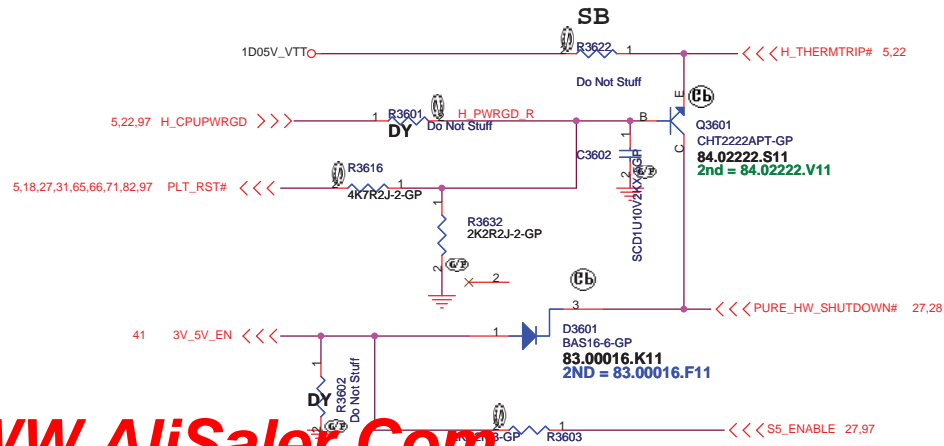
ANNIE Run Power



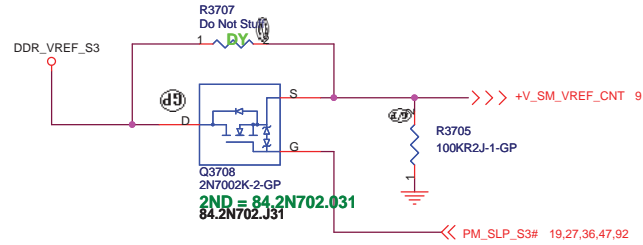
-1 co-layout SLG55221



1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

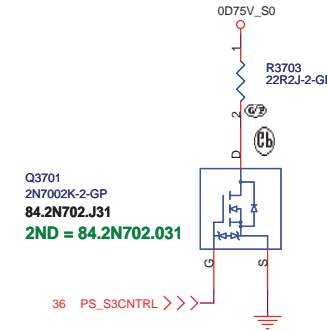


Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

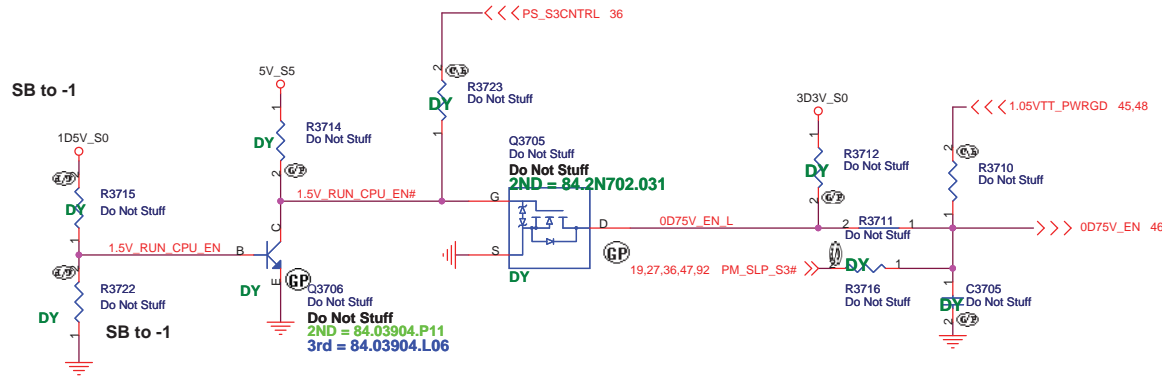


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

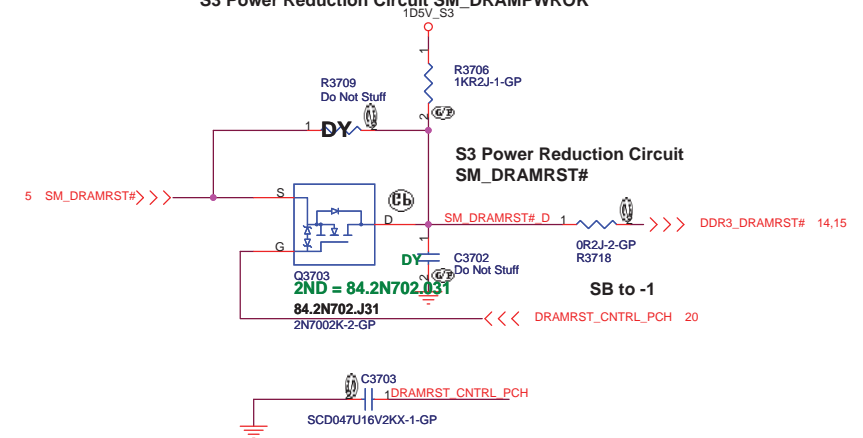
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



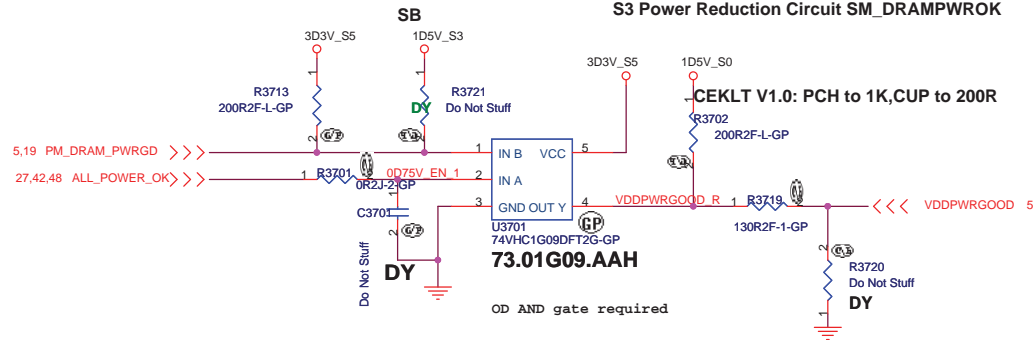
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

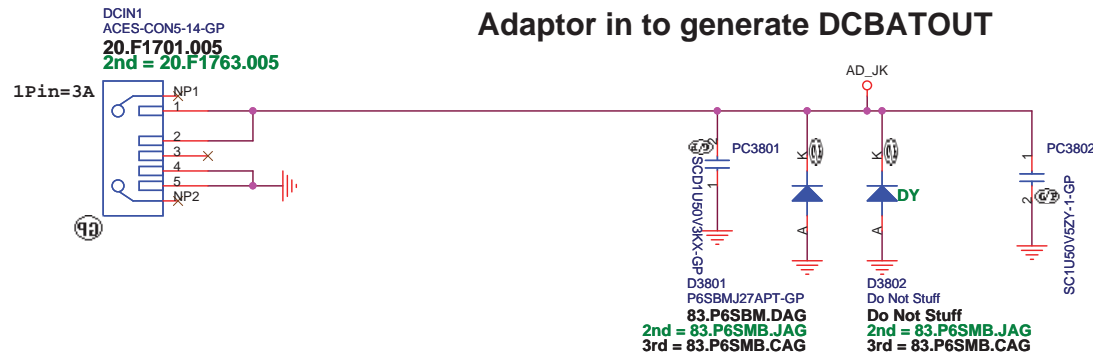
HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

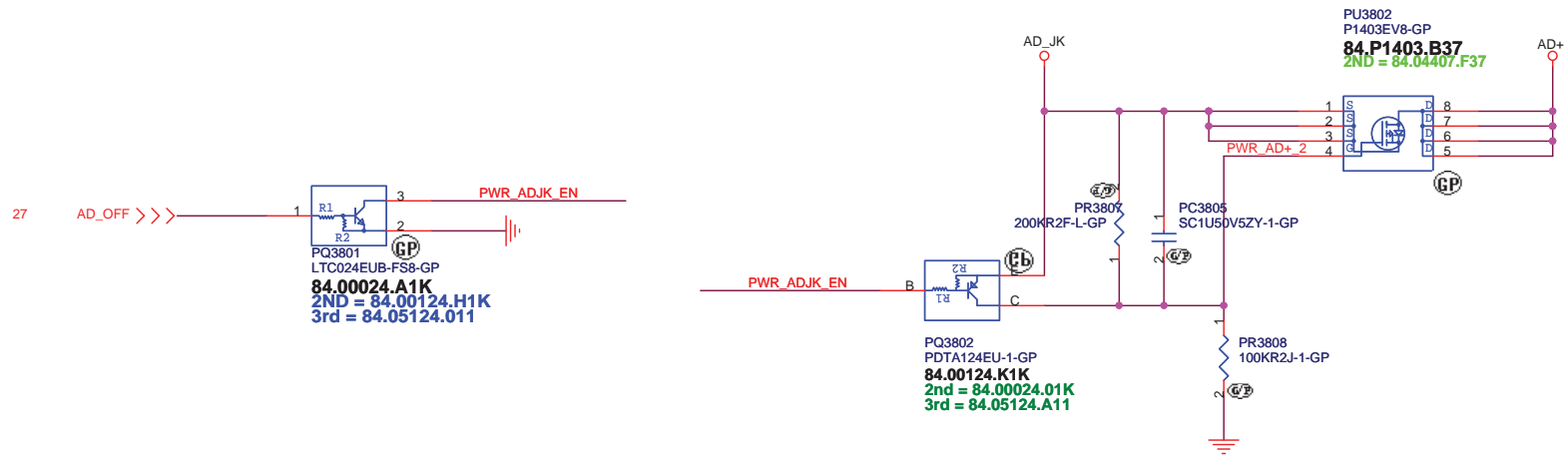
Title ADAPTER		
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 37	of 102

ANNIE solution

Adaptor in to generate DCBATOUT



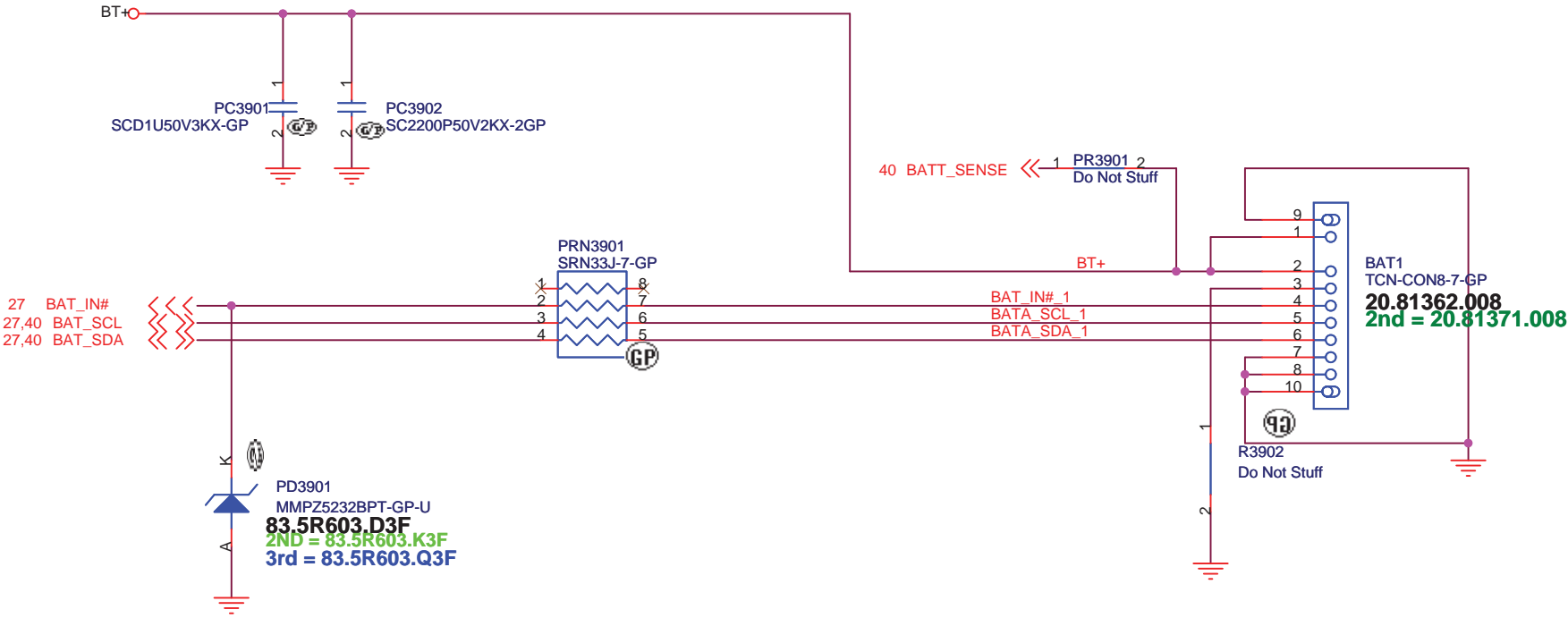
JE40 change DCIN1 part number



HR UMA

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DCIN JACK			
Size	Document Number		Rev
Custom	JE40-HR		-1
Date:	Thursday, December 02, 2010		Sheet 38 of 102

BATTERY CONNECTOR

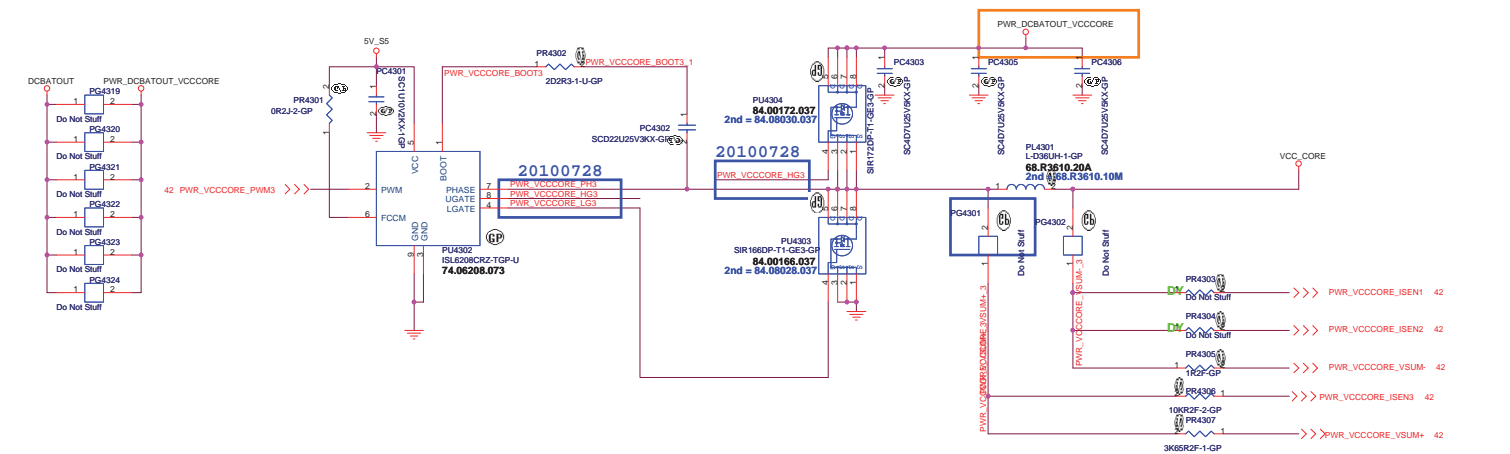
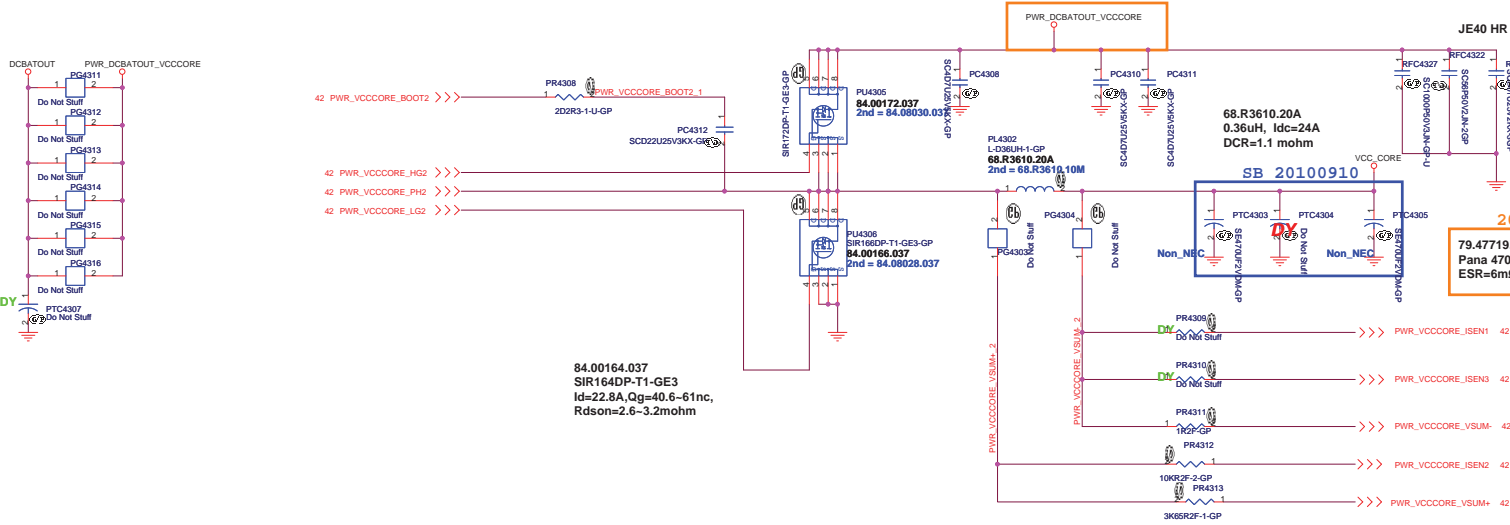
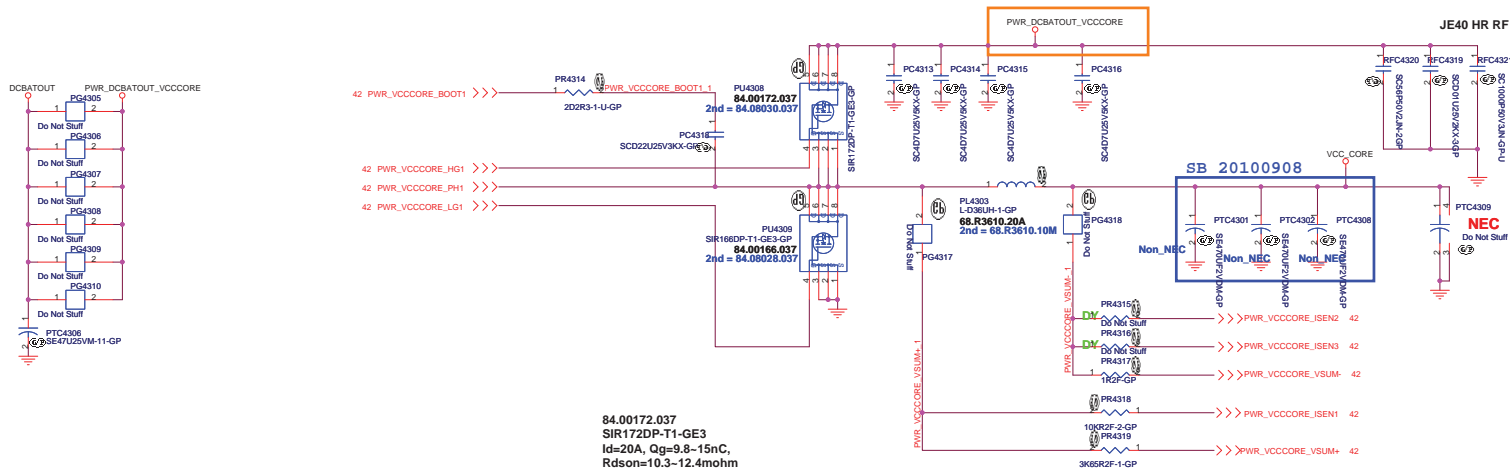


EC Protect

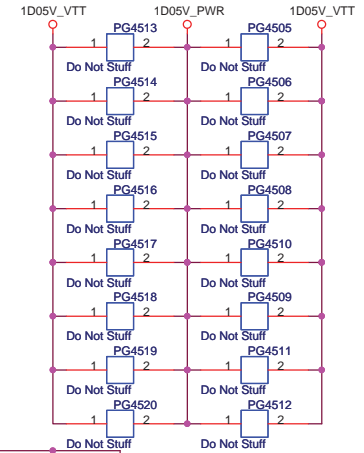
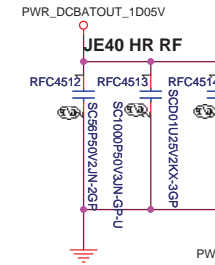
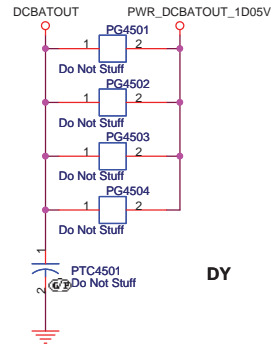
HR UMA

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
BATT CONN			
Size A4	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010		Sheet 39	of 102

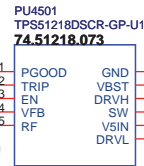
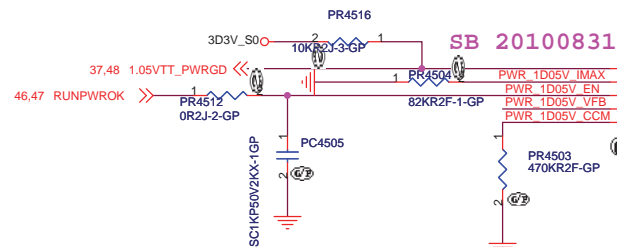




TPS51218D for 1D05V



2nd source 還未導入 74.08237.073



Freq=360KHz

20100728
Id=12.9A
Qg=9.8~15nC
Rdson=10.3~12.4mohm

PU4502
84.15N03.037
2nd = 84.08065.037

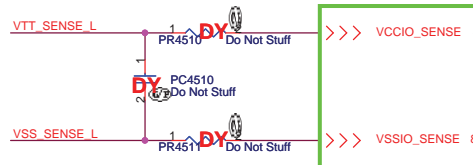
20100728
Iomax=14A
OCP>21A

Mag. 0.56uH 10*10*4
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

20100906
PL4501
IND-D56UH-27-GP
68.R5610.10P
2nd = 68.R5610.20H

PTC4502
Do Not Stuff
2nd = 77.C3371.0512nd = 77.C3371.051

20100728
Id=19.4A
Qg=16.8~25.5nC
Rdson=4.9~6.1mohm



20100728
Vout=0.704*(1+R1/R2)

PTC4503
SE330U2VDM-L-GP
79.33719.L01
2nd = 77.C3371.0512nd = 77.C3371.051

20100728
PR4508
20KR2F-L-GP

20100728
PR4509
10R2F-L-GP

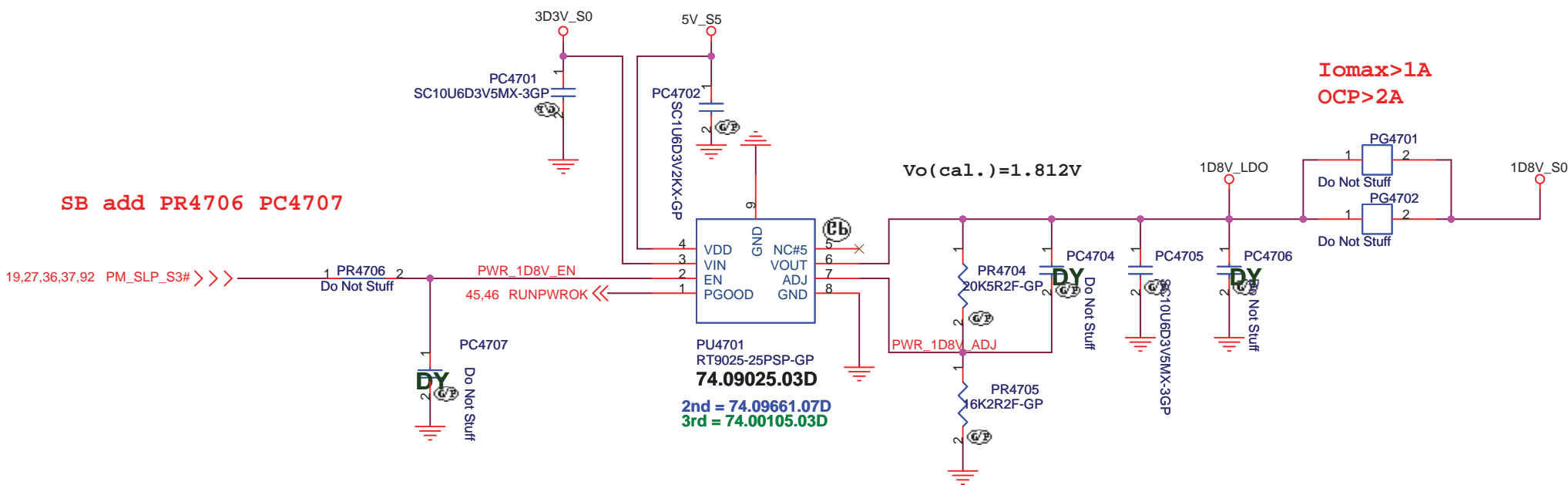
HR UMA

WWW.AliSaler.Com



SSID = PWR.Plane.Regulator_1p8v

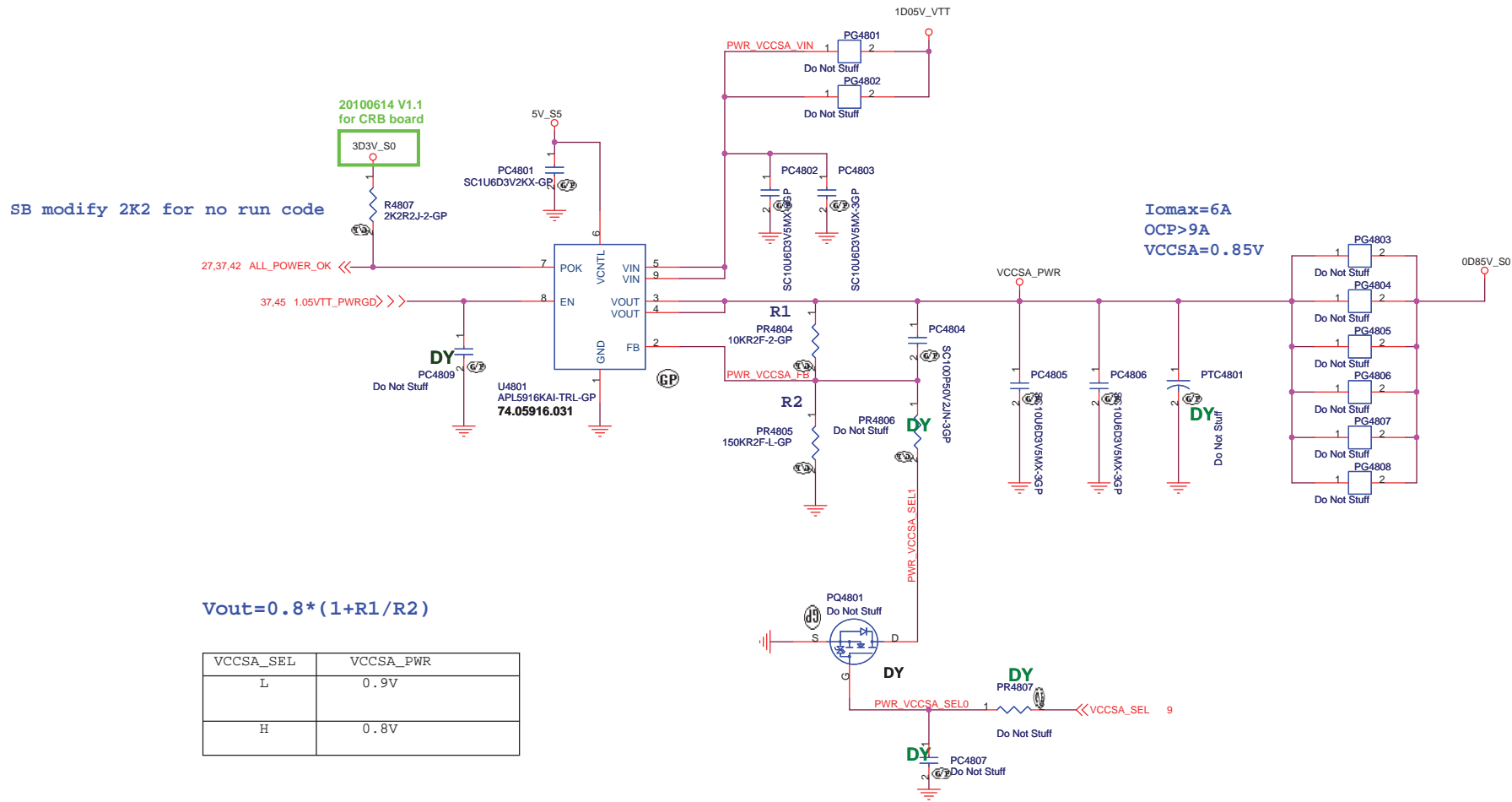
RT9025 for 1D8V_S0



HR UMA

<div>緯創資通</div>		<div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
Title			
<div>LDO 1D8V(RT9025)</div>			
Size A4	Document Number <div>JE40-HR</div>		Rev <div>-1</div>
Date:	Thursday, December 02, 2010	Sheet 47 of	102

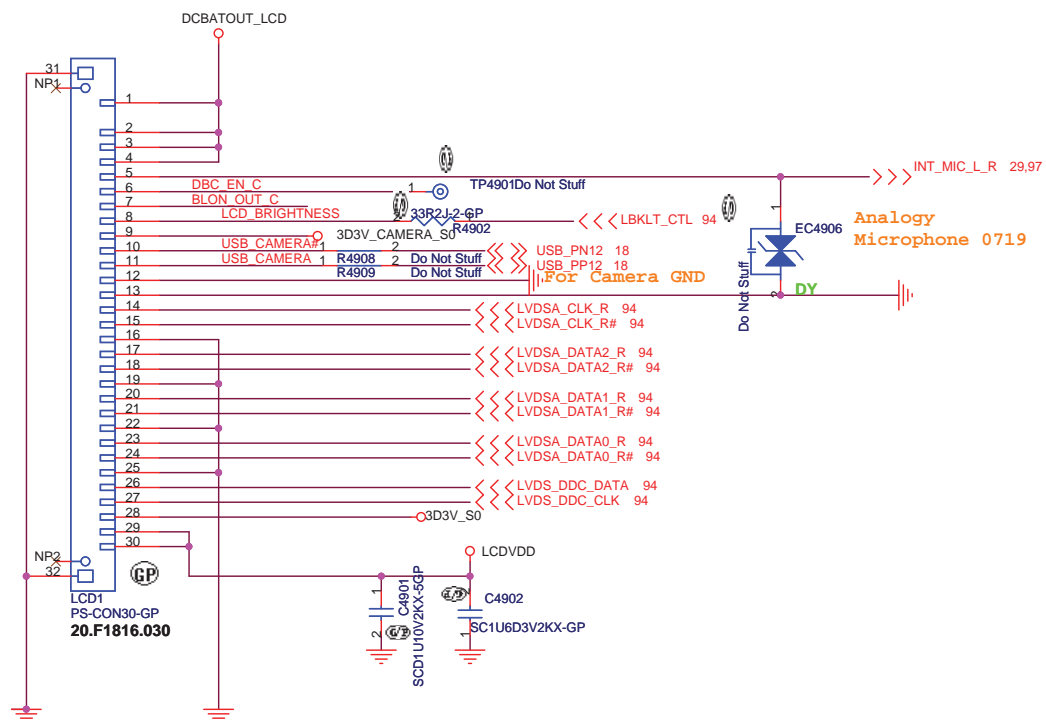
APL5916 for VCCSA



VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

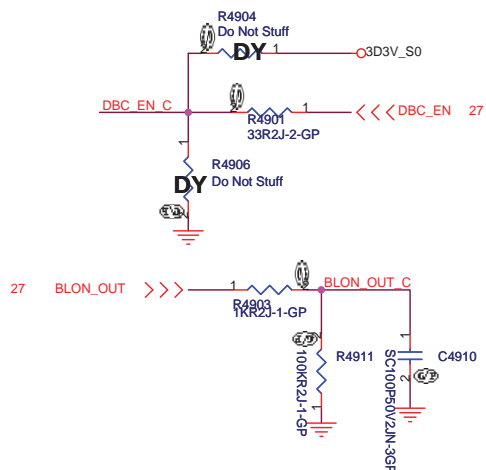
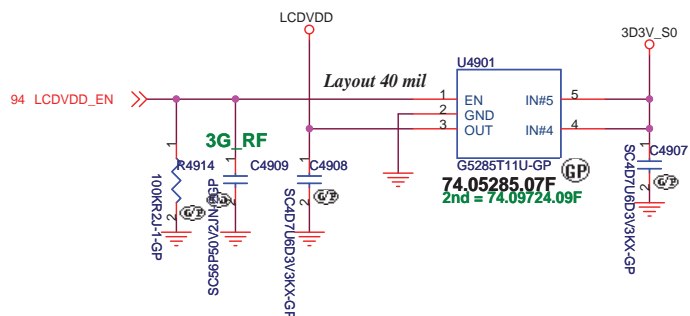
SSID = VIDEO

LVDS CONNECTOR

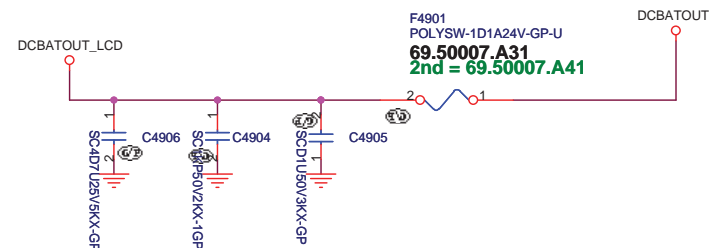


SSID = VIDEO

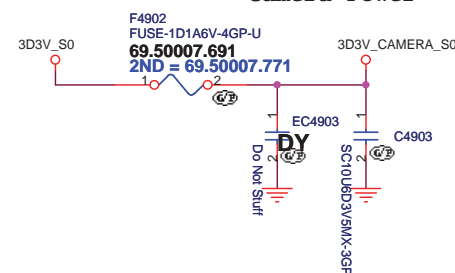
LCD POWER for ANNIE



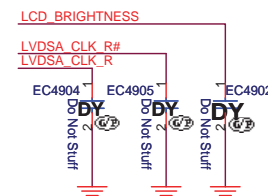
INVERTER POWER



Camera Power



For EMI request
Close to LVDS connector



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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title

LCD Connector

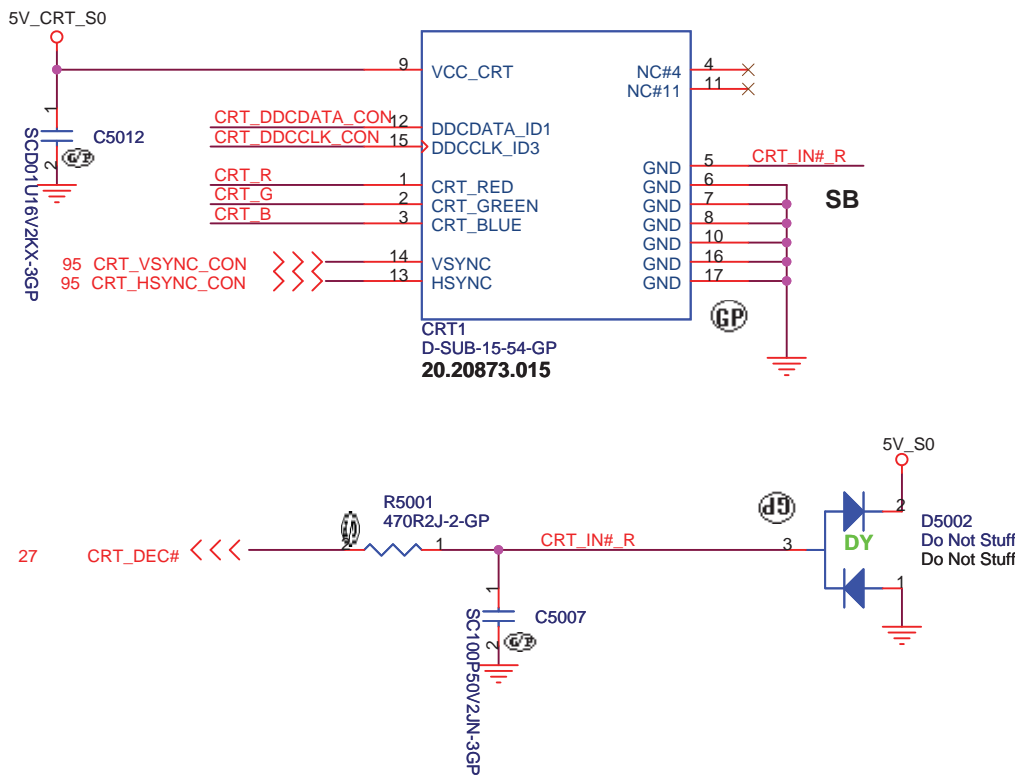
Size	Document Number
------	-----------------

JE40-HR

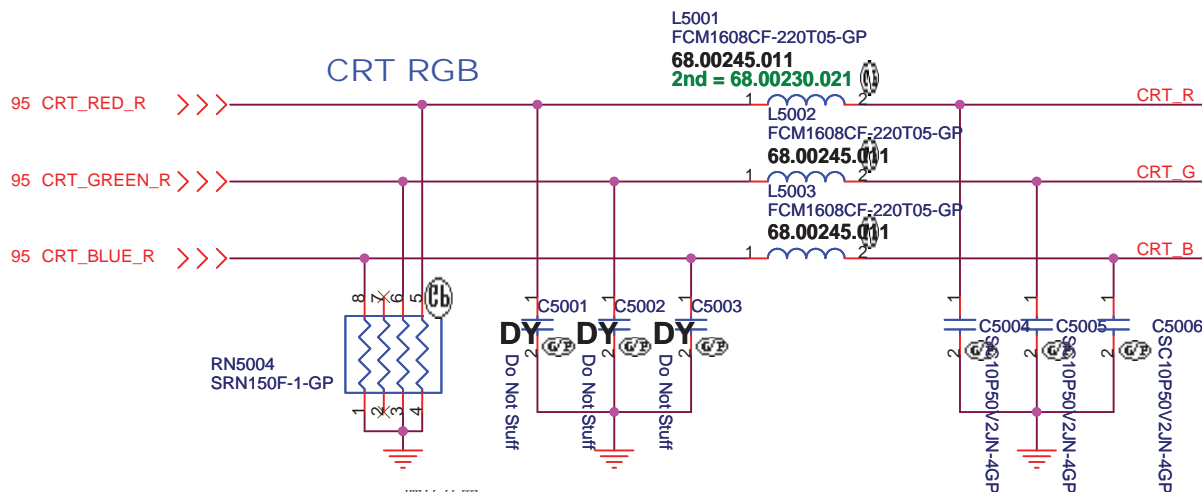
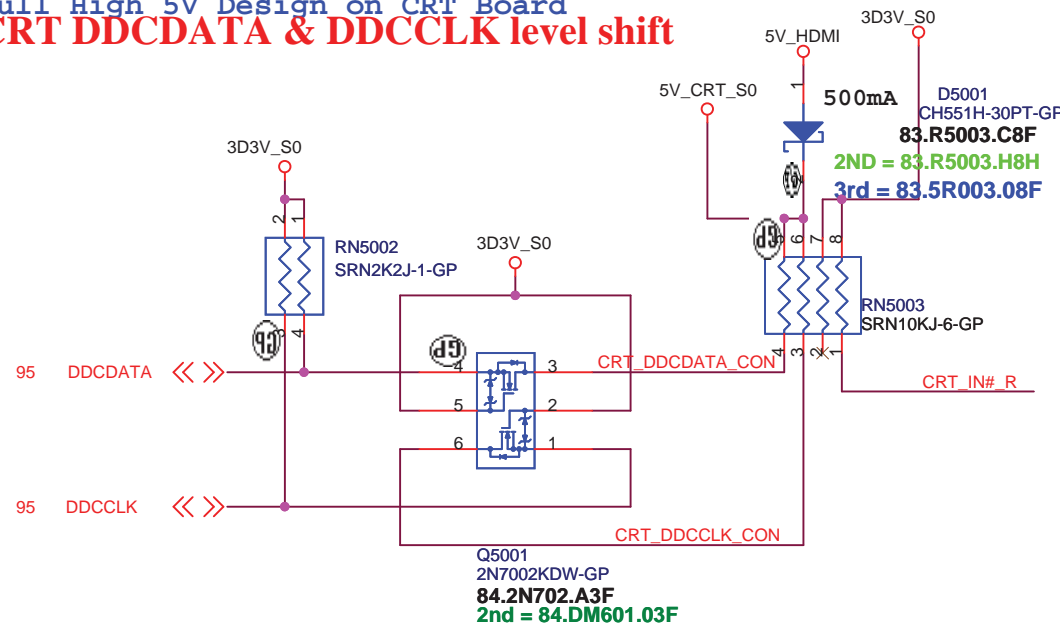
Date: Thursday, December 02, 2010

Sheet 49 of

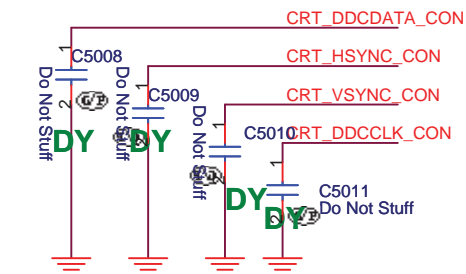
Rev	-1
-----	----



Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift



0806 check RN5004 擺放位置



HR UMA

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size

Document Number

JE40-HR

Rev

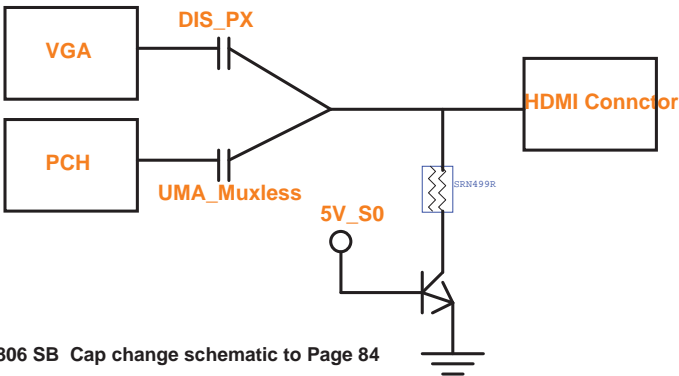
-1

Date: Thursday, December 02, 2010

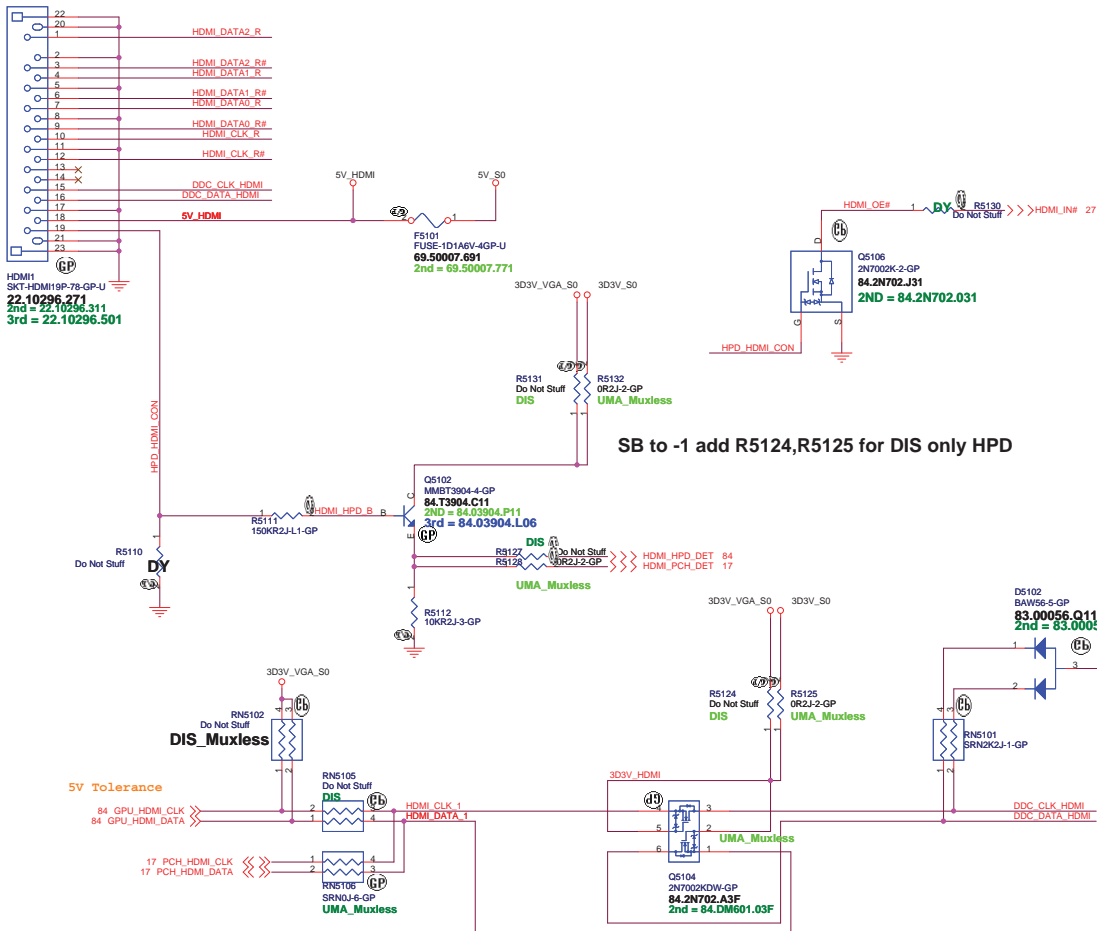
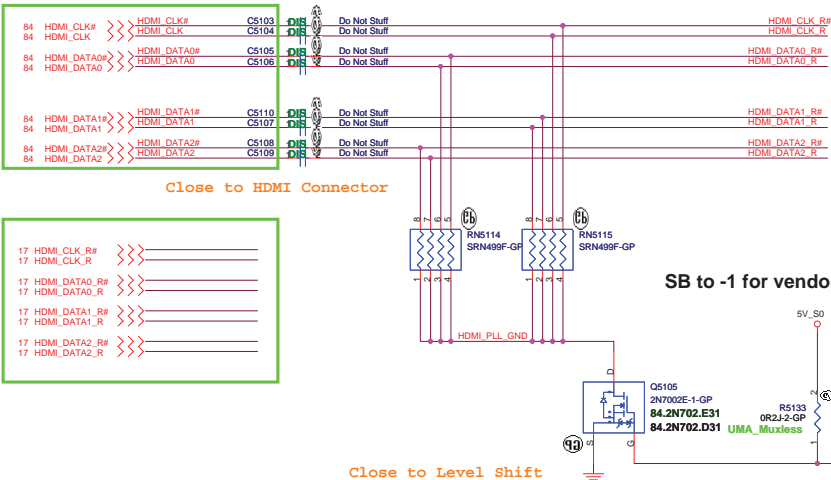
Sheet 50 of 102

HDMI CONN

HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



 <div> 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C. </div>	
HDML Level Shifter/Connector	
Title HDML Level Shifter/Connector	Rev -1
Size Custom	Document Number JE40-HR
Date Thursday, December 02, 2010	Sheet 51 of 102

HR UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

eDP

Size
A3

Document Number
JE40-HR

Rev
-1

Date: Thursday, December 02, 2010

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(Blanking)

HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
S-VIDEO		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 53 of 102

(Blanking)

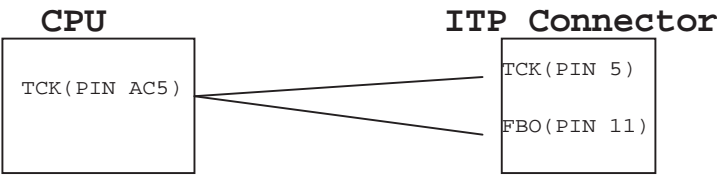
HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

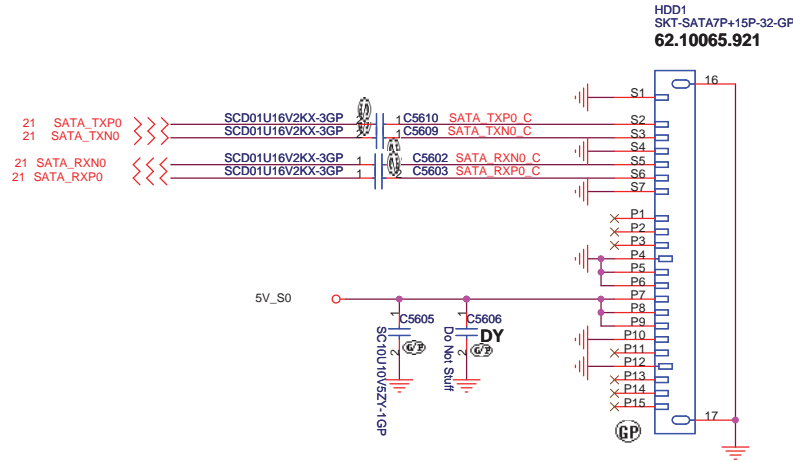


HR UMA

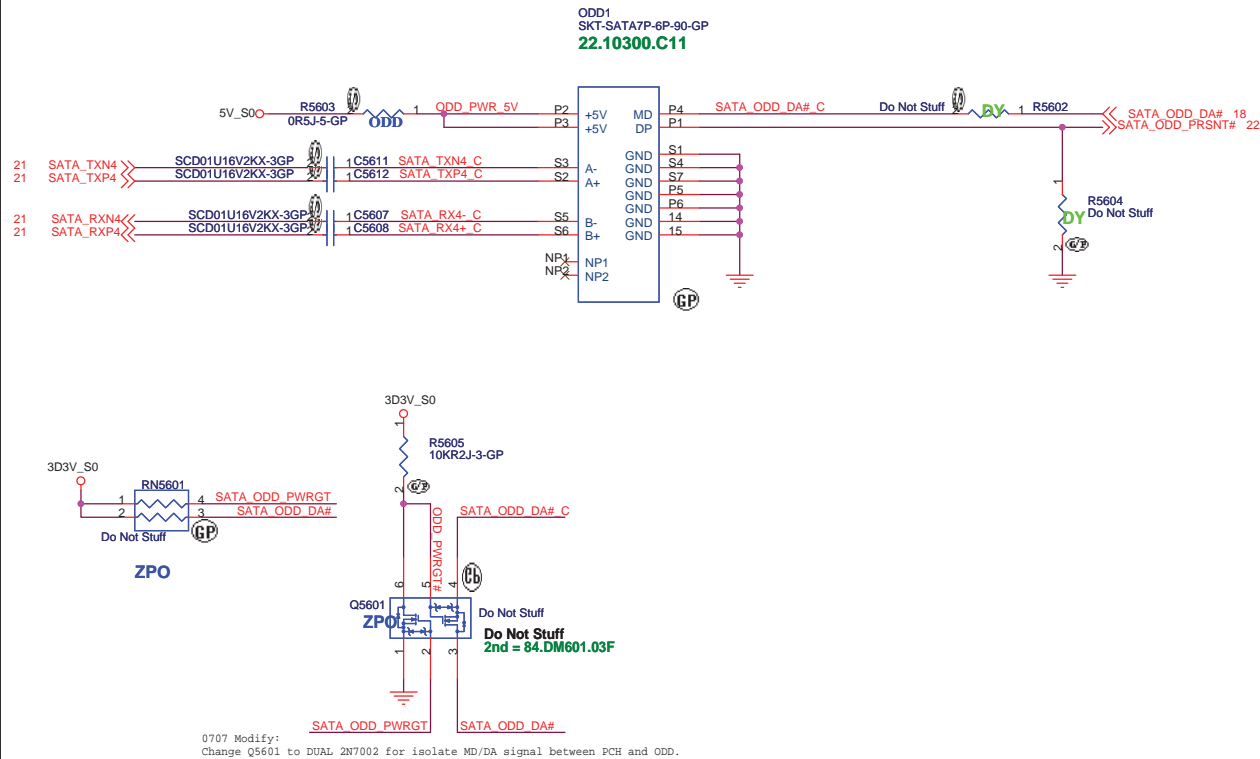
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ITP			
Size A4	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010		Sheet 55 of	102

SSID = SATA

SATA HDD Connector



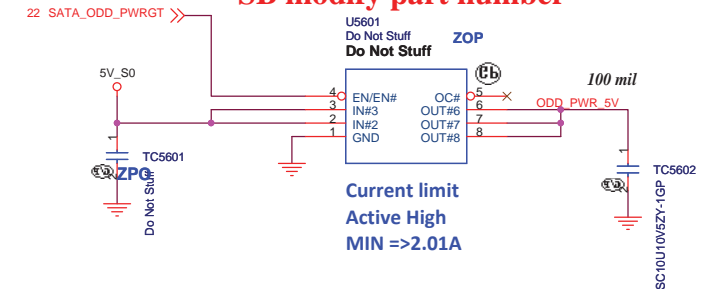
ODD Connector



SB

SATA Zero Power ODD

SB modify part number



HR UMA

緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
HDD/ODD		
Size A3	Document Number	Rev
	JE40-HR	-1
Date: Thursday, December 02, 2010	Sheet 56	of 102

ESATA Power

USB CHARGER

HR UMA

緯創資通

Wistron Corporation

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Title

Size
A3

Document Number
JE40-HR

Date: Thursday, December 02, 2010

E-SATA/USB CHARGER

Rev
-1

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SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

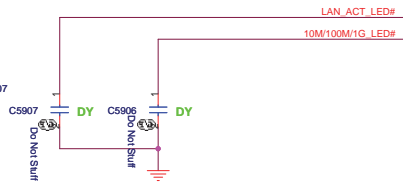
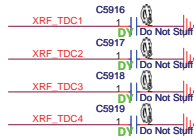
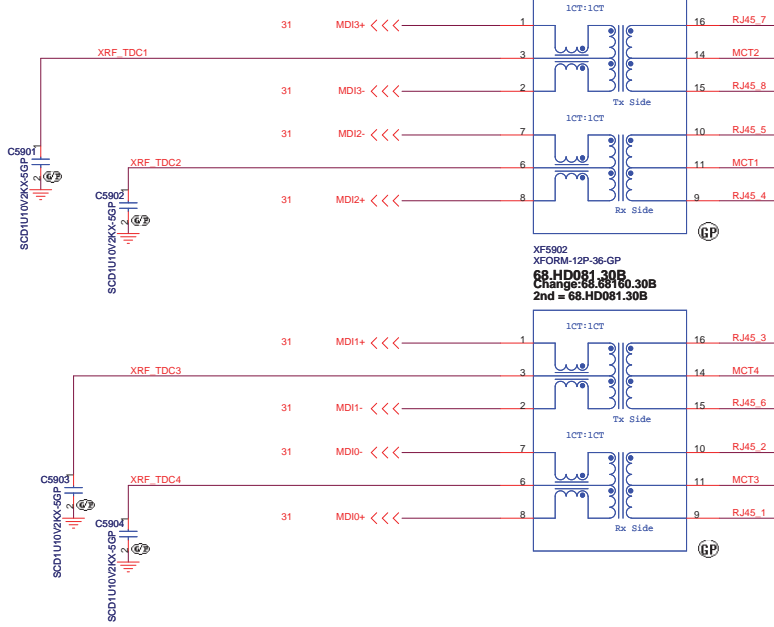
JE40 delete Line in function

SSID = LOM

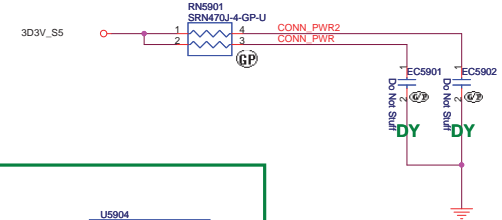
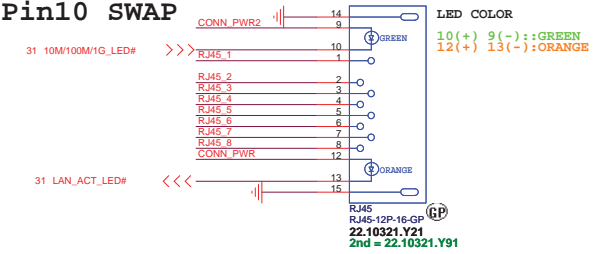
GIGA Lan Transformer

XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.88160.30B
2nd = 68.HD081.30B

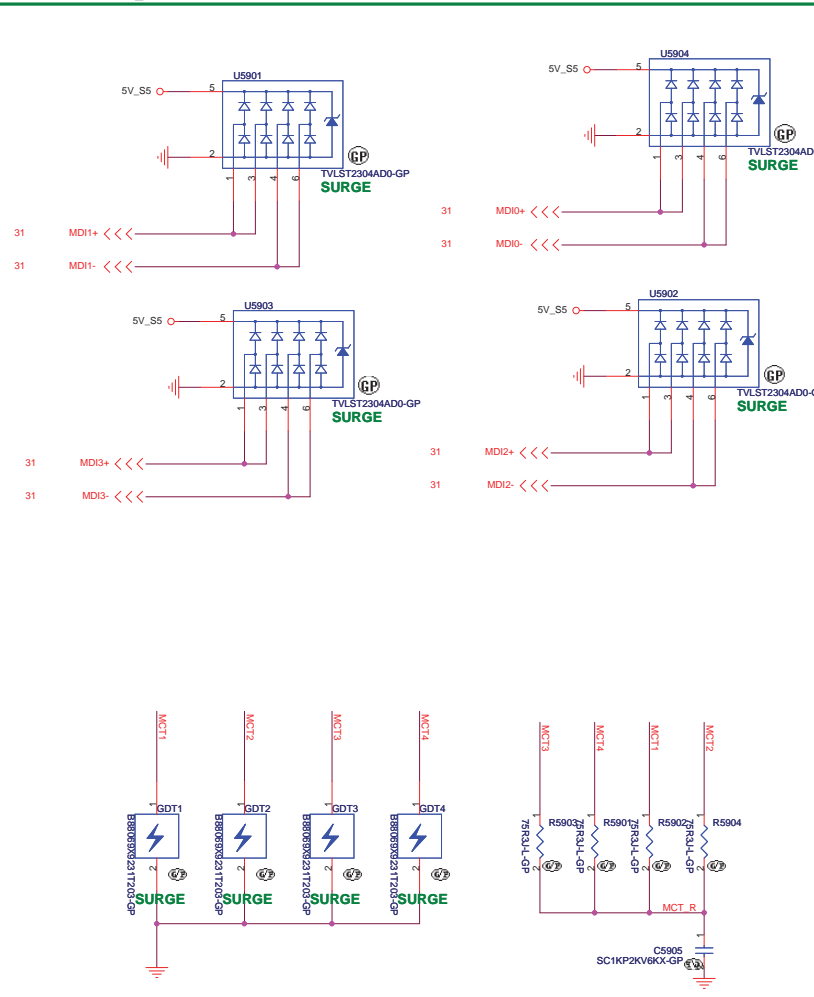
LAN MDI Off-Page



SB modifyf Pin9 Pin10 SWAP



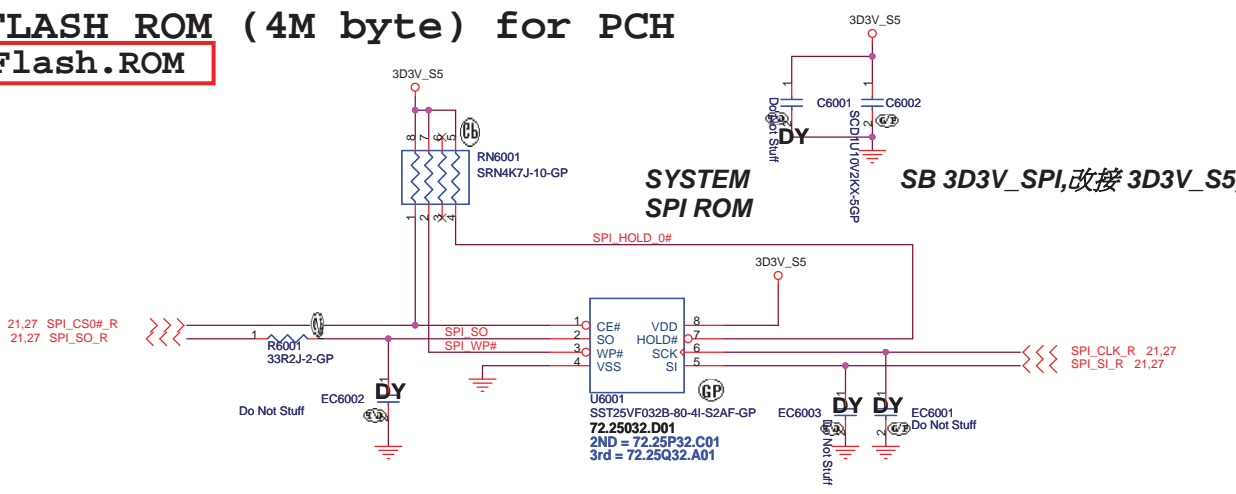
SB modify For EMI



HR UMA

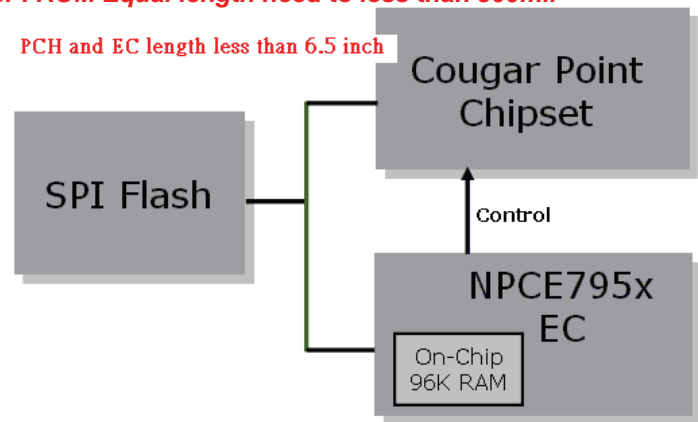
SPI FLASH ROM (4M byte) for PCH

SSID = Flash.ROM

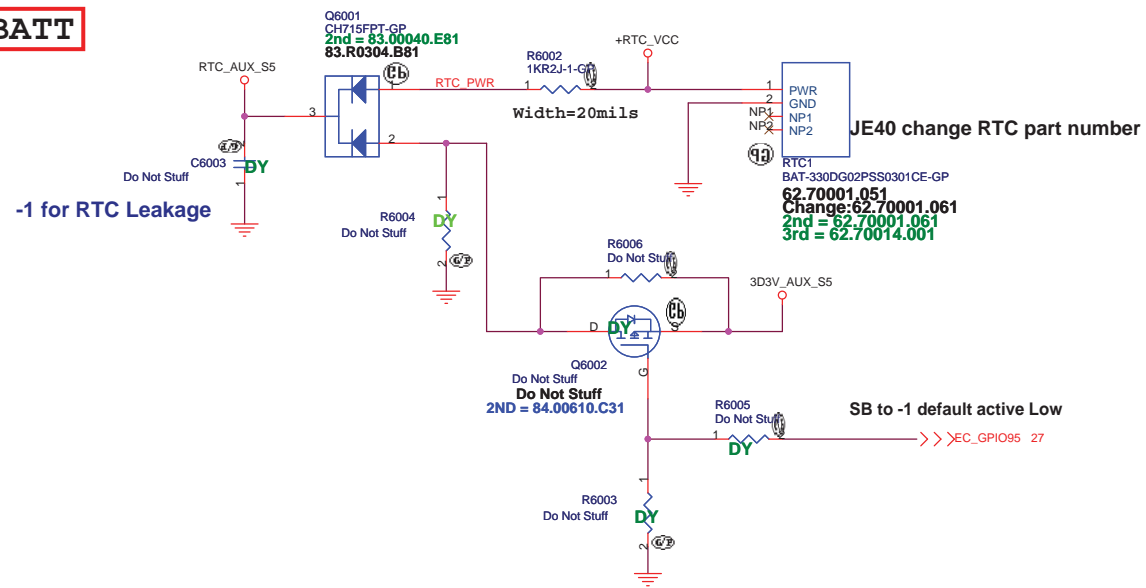


SPI ROM Equal length need to less than 500mil

PCH and EC length less than 6.5 inch



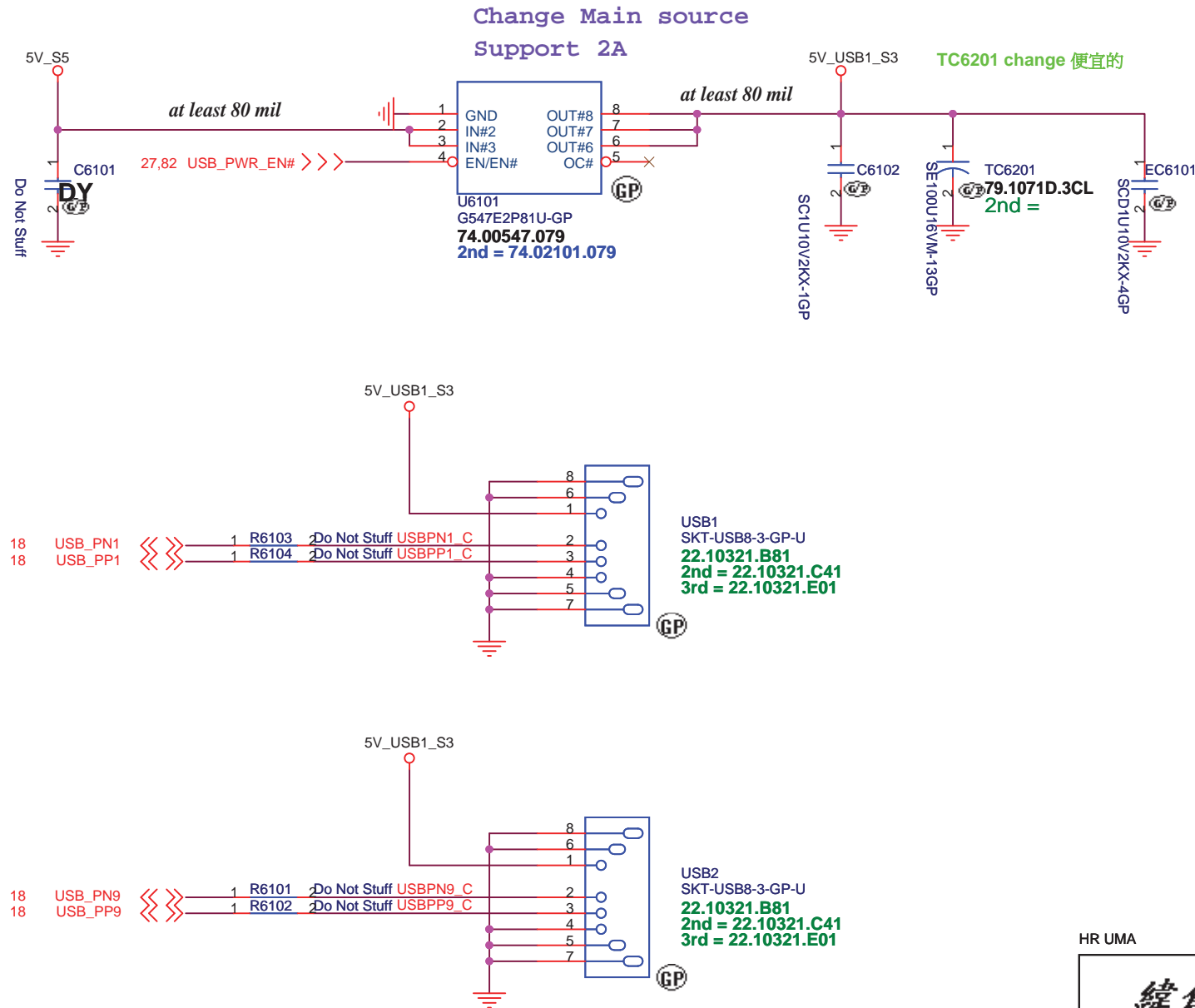
SSID = RBATT



HR UMA			
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Flash/RTC			
Size	Document Number		Rev
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SSID = USB

IO Board USB Power



HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size
A4

Document Number

JE40-HR

Rev
-1

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HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

USB 3.0 Port

Size
A3

Document Number
JE40-HR

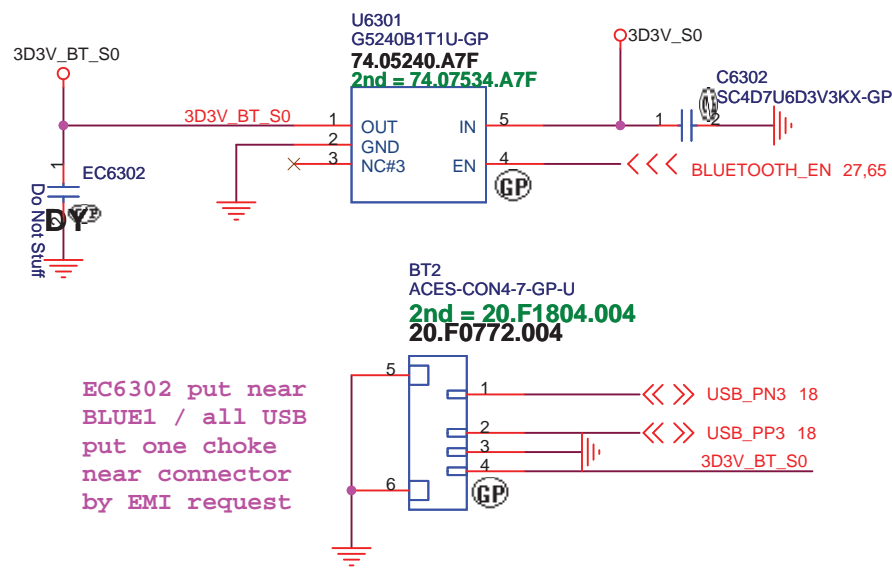
Date: Thursday, December 02, 2010

Rev
-1

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SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module



HR UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Bluetooth			
Size	Document Number	Rev	
A4	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	63 of 102

Finger printer

JE40 delete FP function

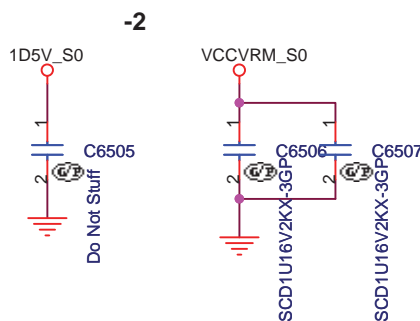
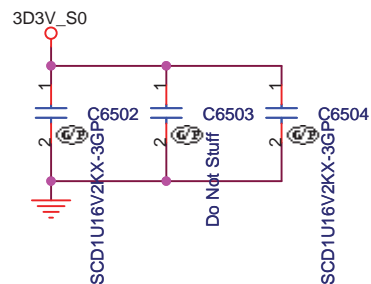
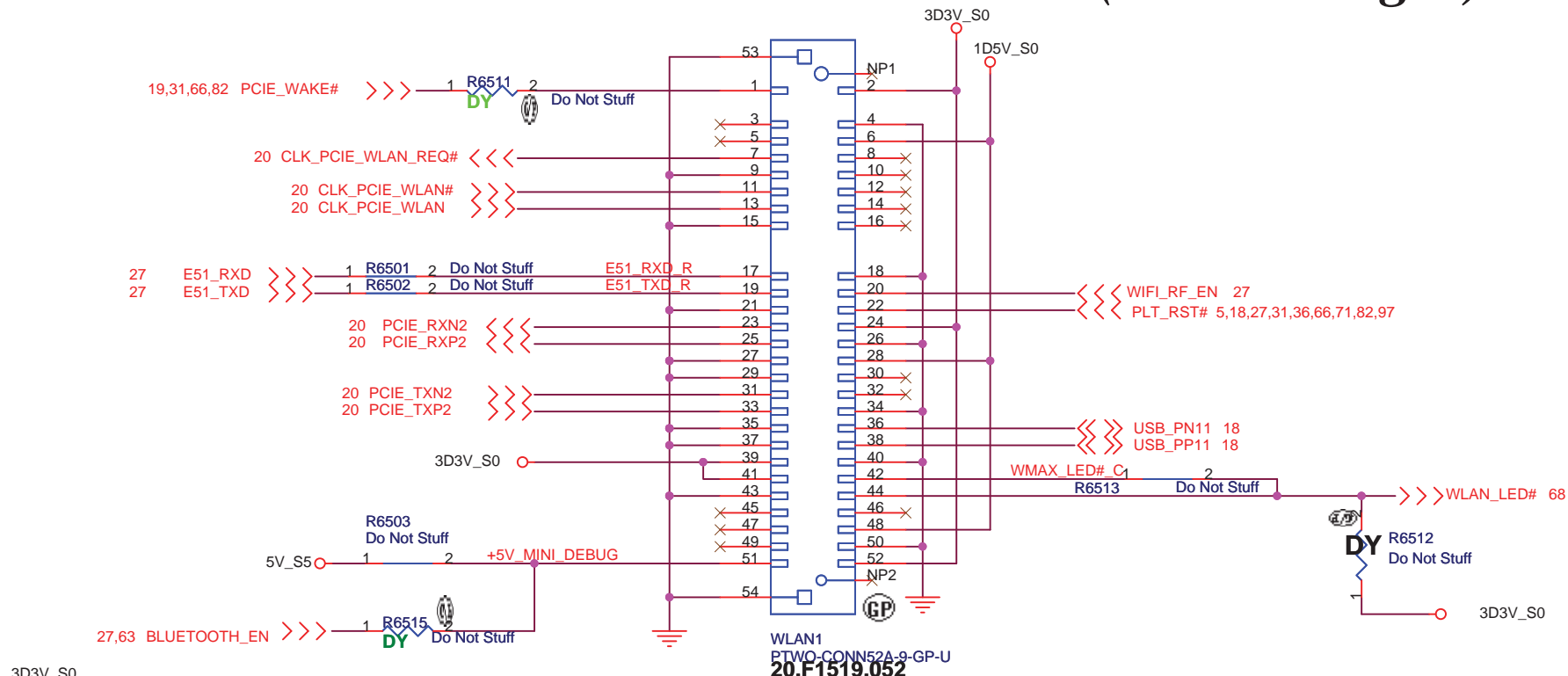


HR UMA

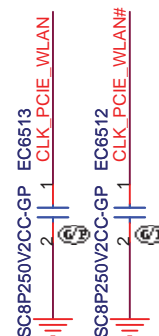
<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title		
RESERVED		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 64 of 102

SSID = Wireless

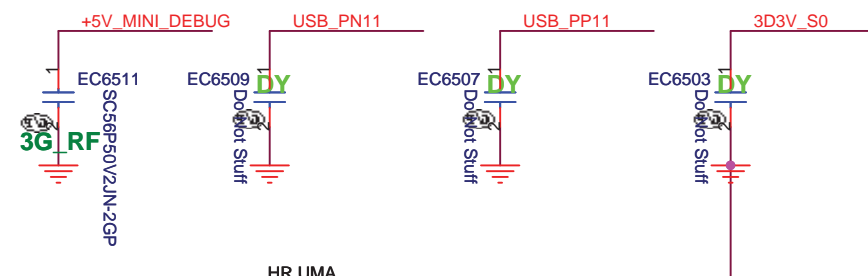
Mini Card Connector(802.11a/b/g/n)



SB modify for SIV



RF suggestion



HR UMA

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

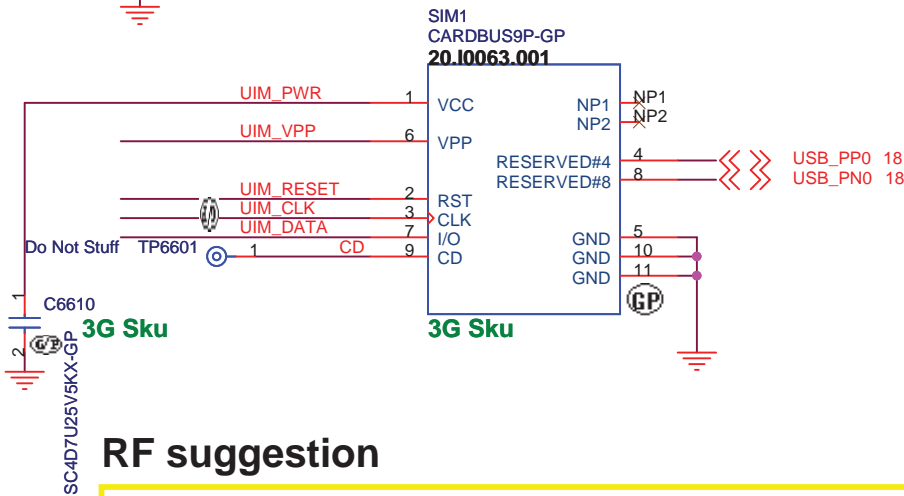
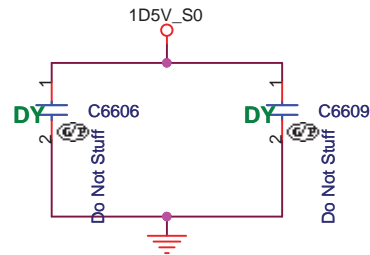
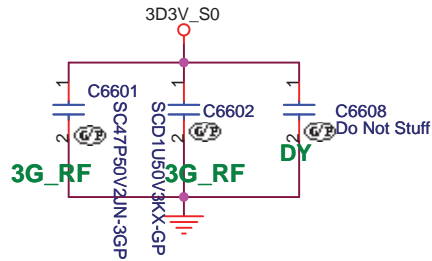
Title		
MINICARD(WLAN)/ITP CONN		
Size	Document Number	Rev
A4	JE40-HR	-1
Date	Thursday, December 02, 2010	Sheet 65 of 102

SSID = Wireless

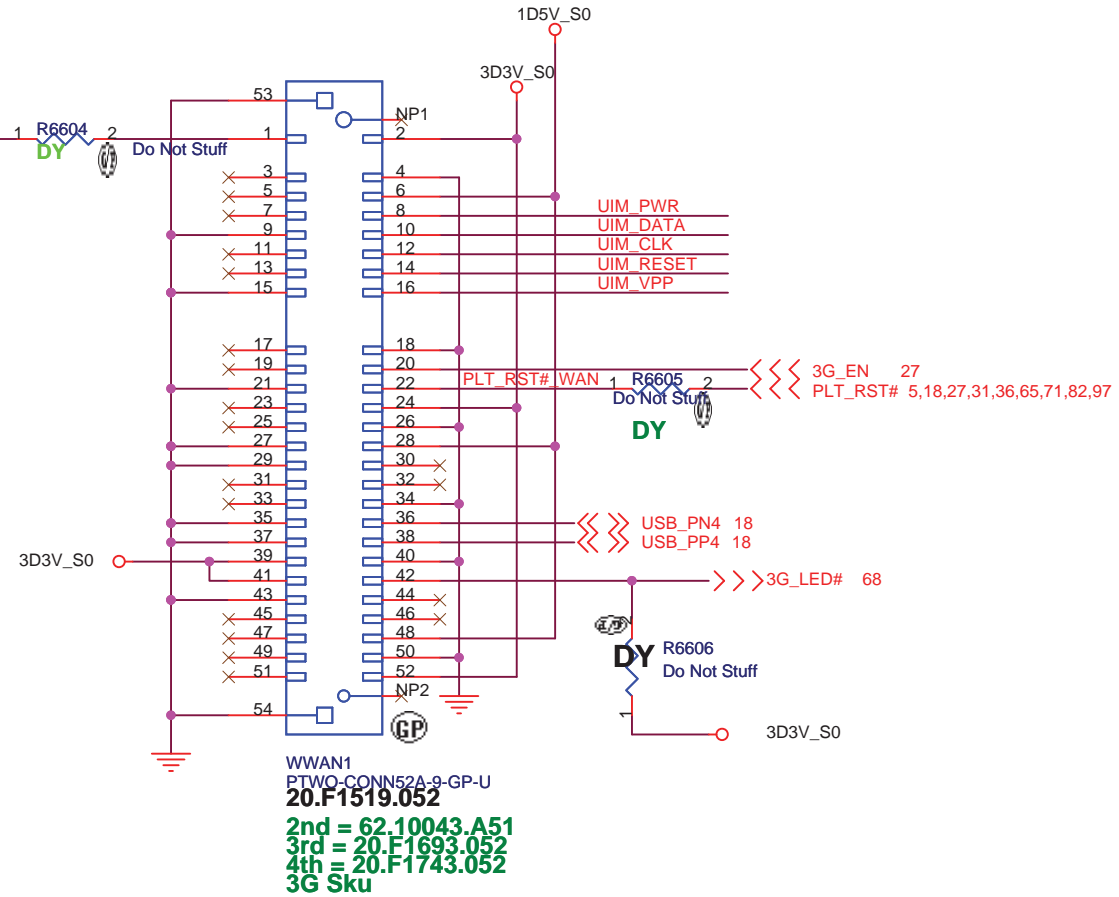
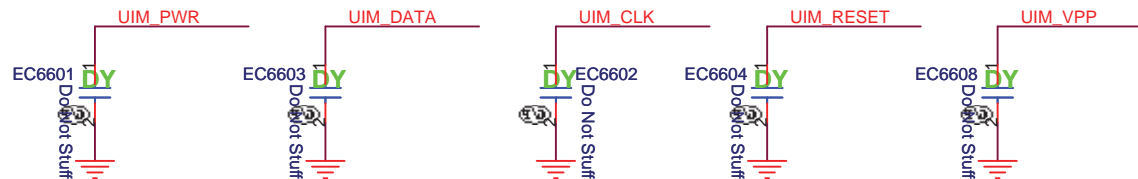
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size

Document Number

JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

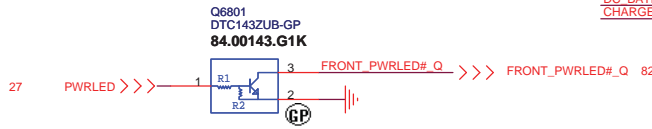
Sheet 66 of 102

(Blanking)

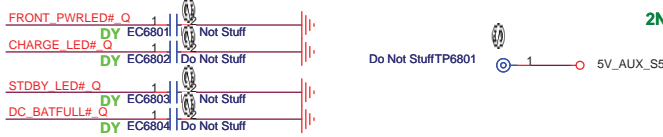
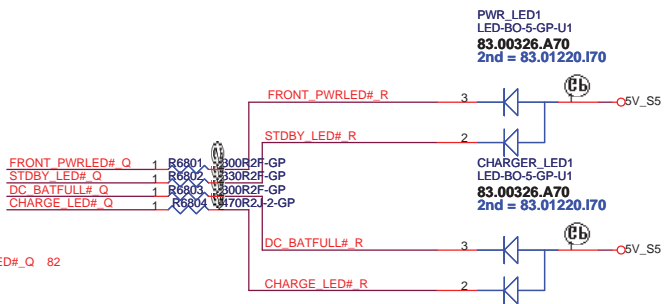
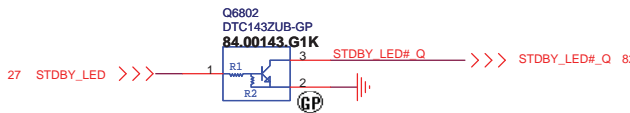
HR UMA

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 67 of 102

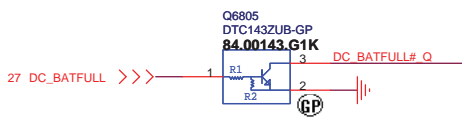
Power button LED



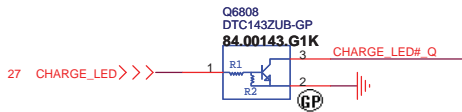
Power STDBY_LED



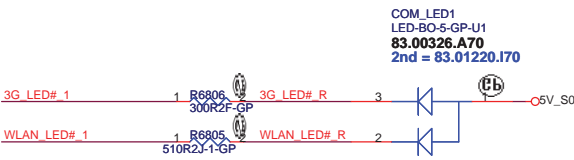
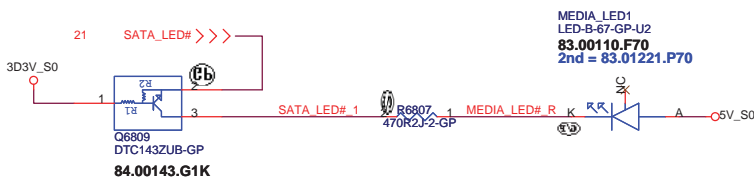
Battery LED2(DC_BATFULL)



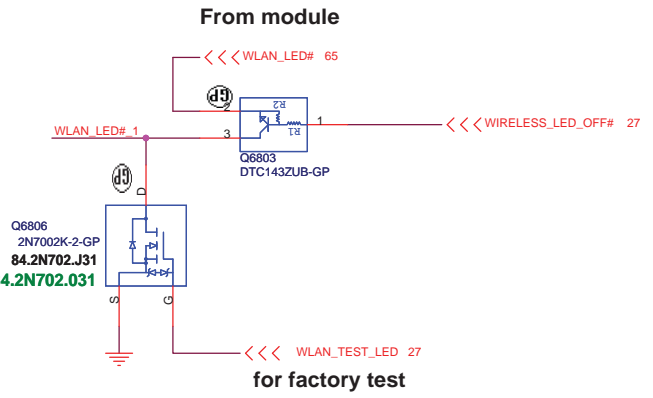
Battery LED1(CHARGE)



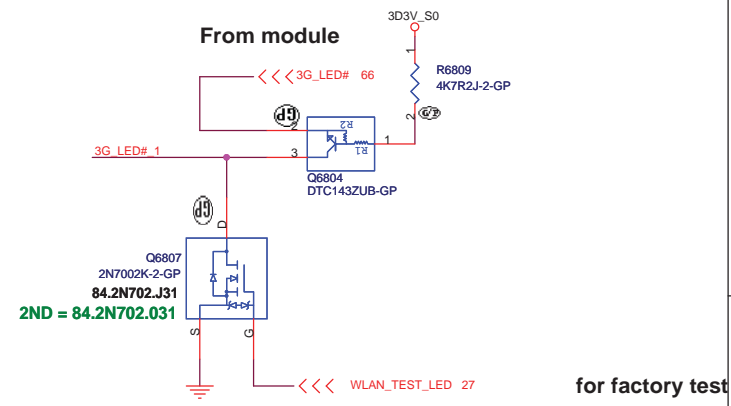
SATA HDD LED



WLAN_LED



3G LED



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

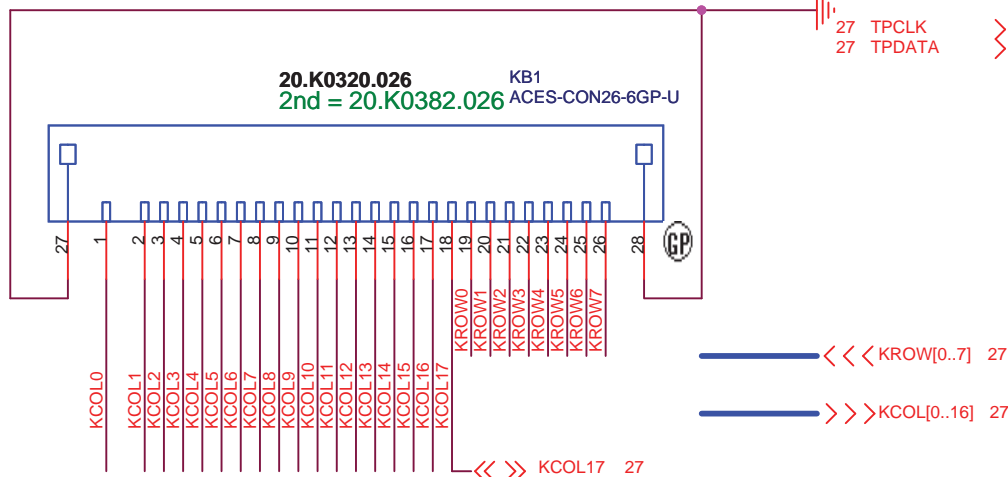
Title: **LED Bard/Power Button**

Size: Custom Document Number: **JE40-HR** Rev: **-1**

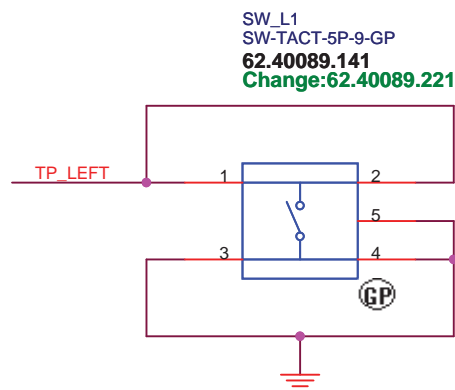
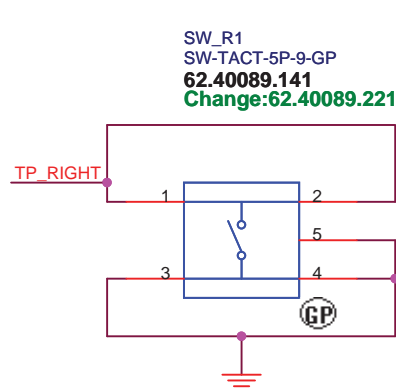
Date: Thursday, December 02, 2010 Sheet: 68 of 102

SSID = KBC

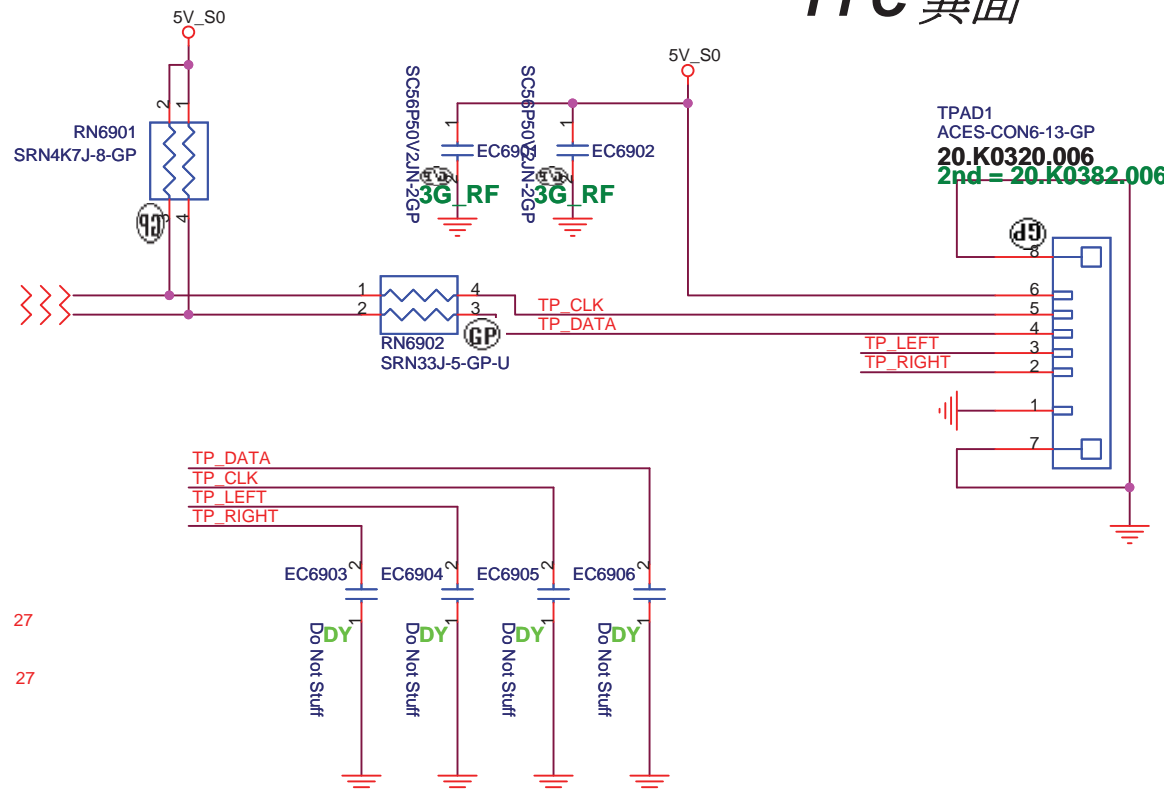
Internal KeyBoard Connector



SB to -1 modify Part number



TOUCH PAD



FFC 異面

HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size

Document Number

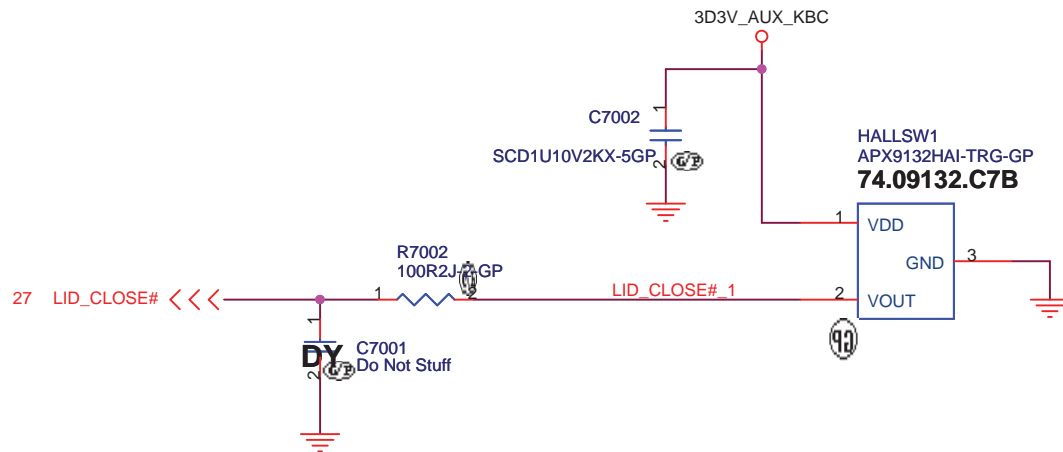
JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

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HR UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

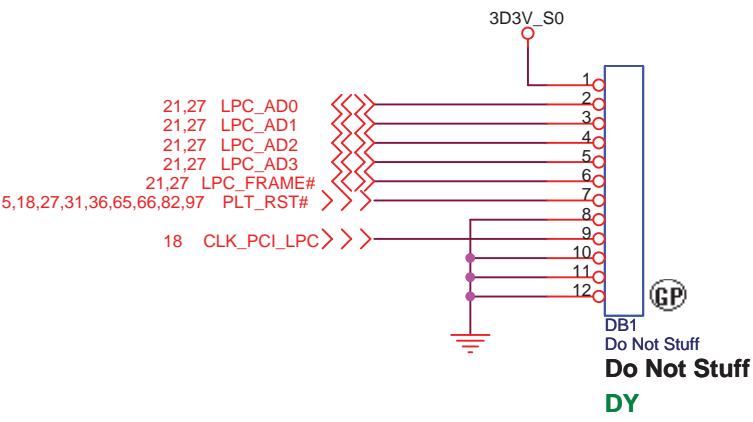
Document Number

JE40-HR


Rev
-1

Date: Thursday, December 02, 2010

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HR UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Dubug connector			
Size A4	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010		Sheet 71 of	102

(Blanking)

HR UMA

<div>緯創資通Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
Reserved		
Size	Document Number	Rev
A3	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 72 of 102

(Blanking)

HR UMA

緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
A3

Document Number
JE40-HR

Date: Thursday, December 02, 2010

Reserved

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-1

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SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

(Blanking)

HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 76 of 102

(Blanking)

HR UMA

<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
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SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

HR UMA

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Title

Free Fall Sensor

Size
A4

Document Number

JE40-HR

Rev
-1

Date: Thursday, December 02, 2010

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HR UMA

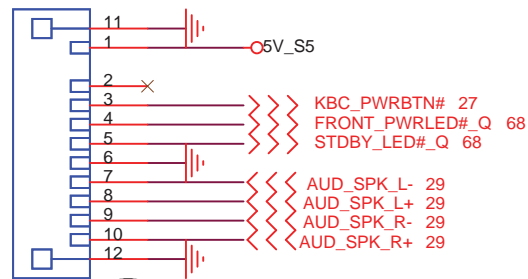
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
Date: Thursday, December 02, 2010		Sheet 80 of 102

(Blanking)

HR UMA

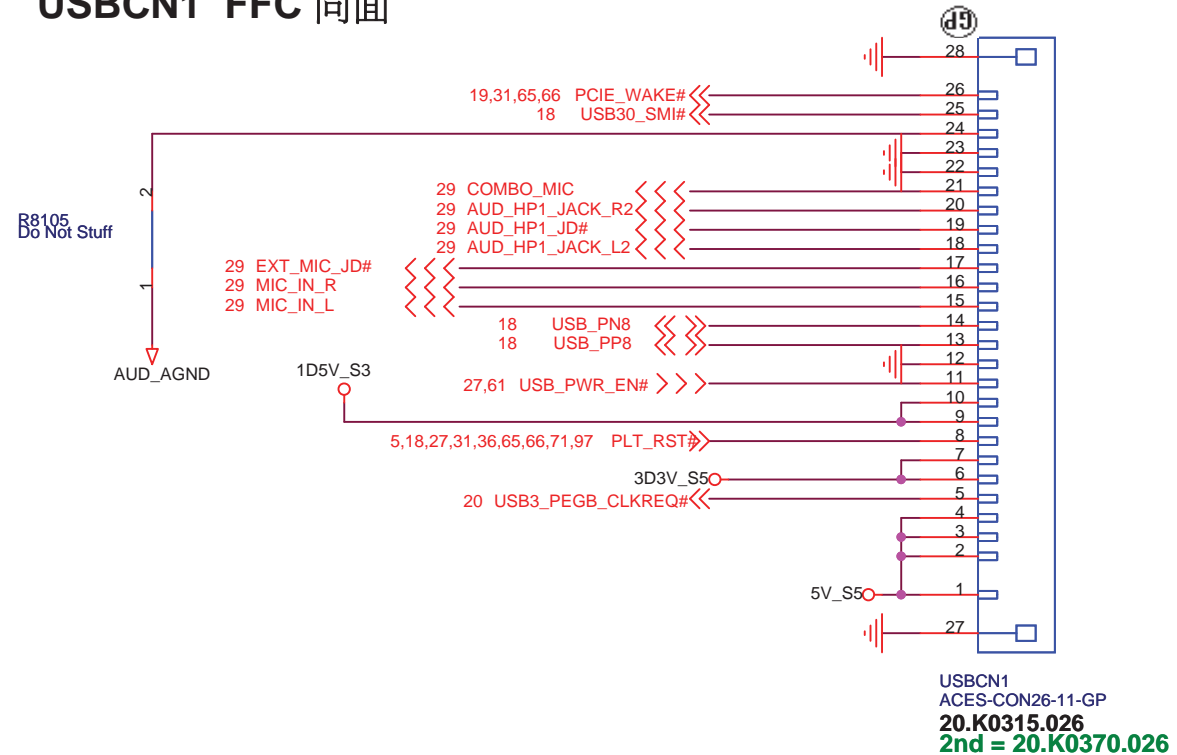
<div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>Reserved</div>		
Size <div>A4</div>	Document Number <div>JE40-HR</div>	Rev <div>-1</div>
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PWRCN1 FFC 異面



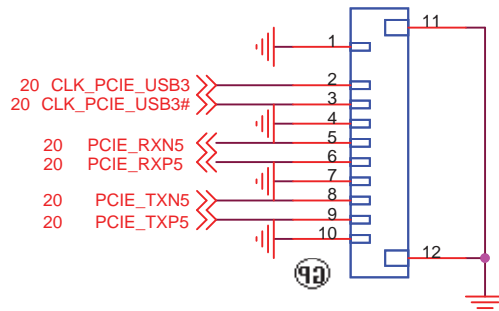
PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

USBCN1 FFC 同面



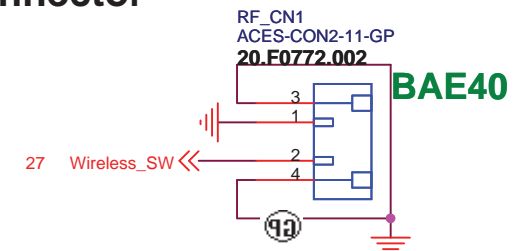
0806 change 10Pin

USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

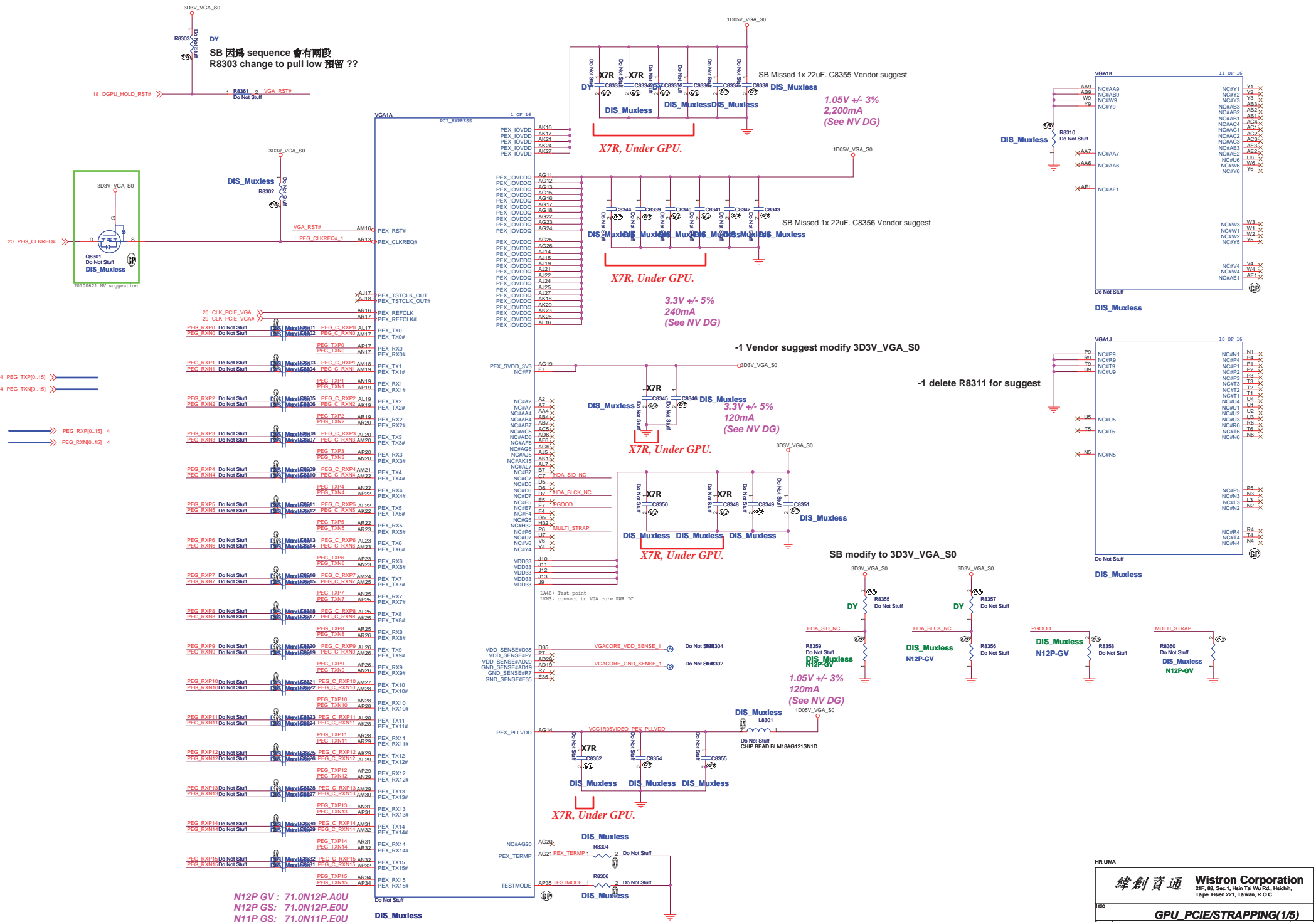
-1 add RF connector
BAE40 Only



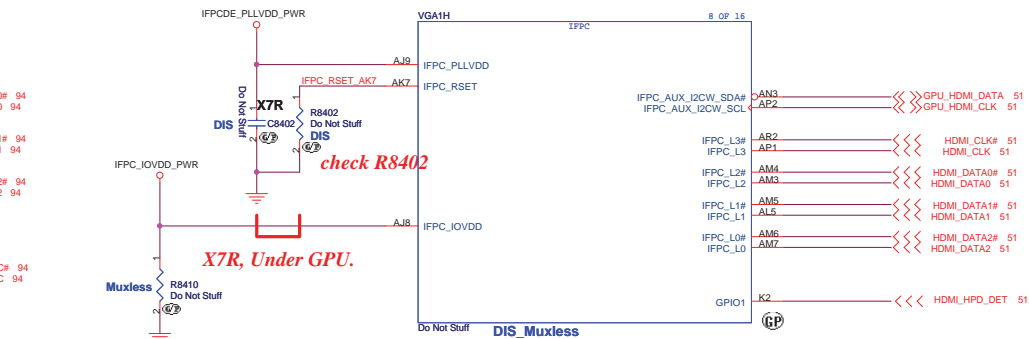
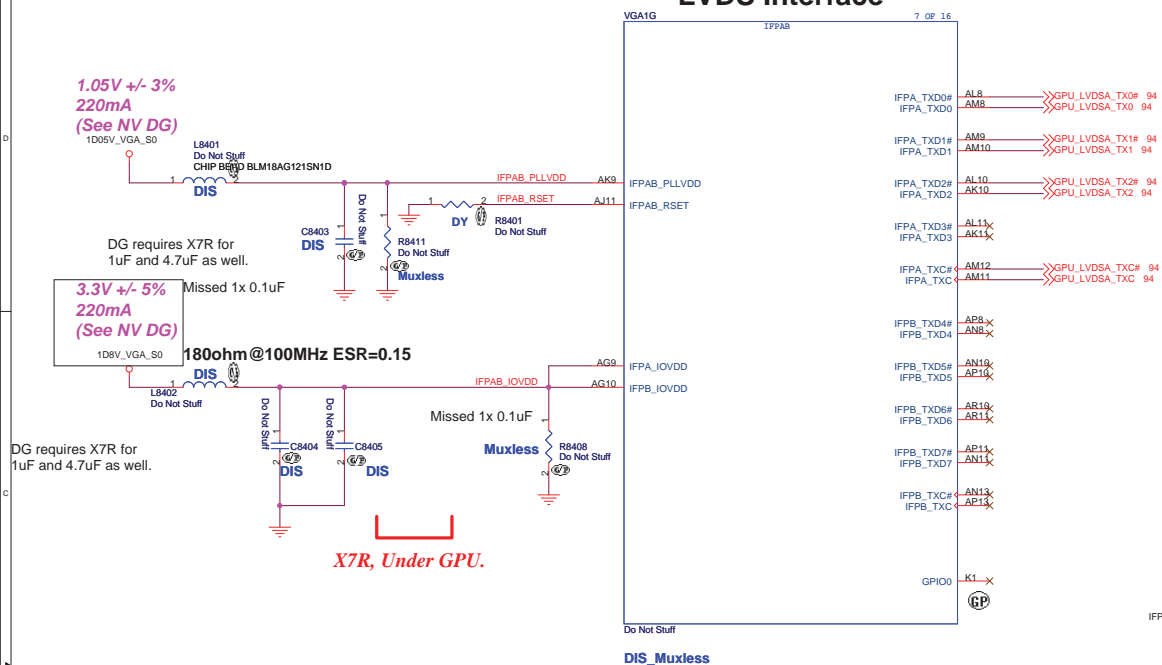
Cabele Wire to BD

HR UMA

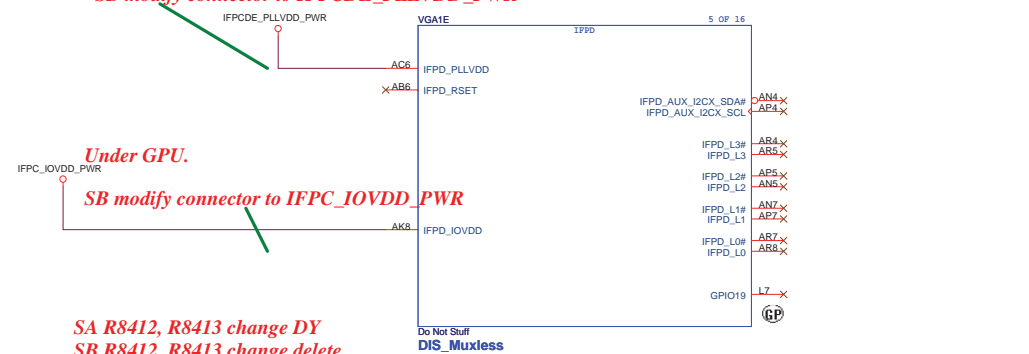
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
IO Board Connector			
Size A4	Document Number JE40-HR		Rev -1
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LVDS Interface



SB modify connector to IFPCDE_PLLVDD_PWR

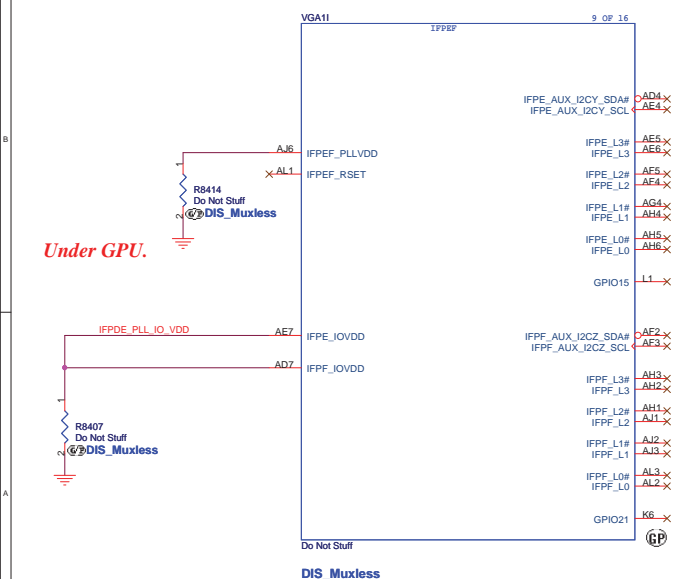


Under GPU.

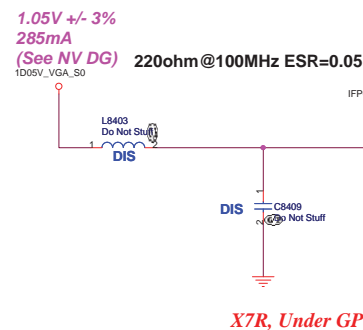
SB modify connector to IFPC_IOVDD_PWR

SA R8412, R8413 change DY
SB R8412, R8413 change delete

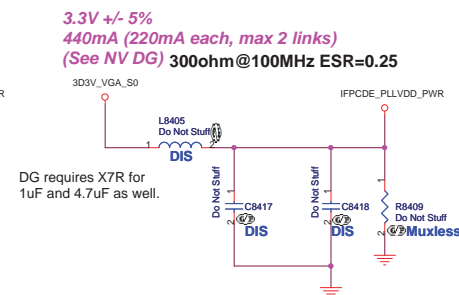
HDMI Interface



Under GPU.



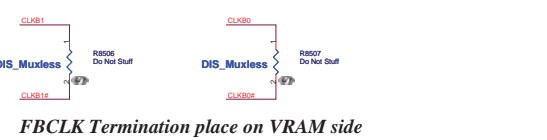
X7R, Under GPU.

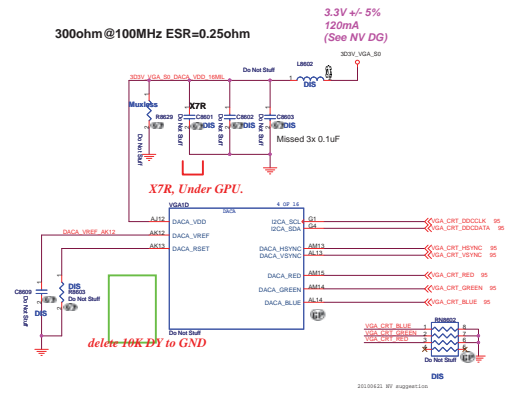


DG requires X7R for 1uF and 4.7uF as well.

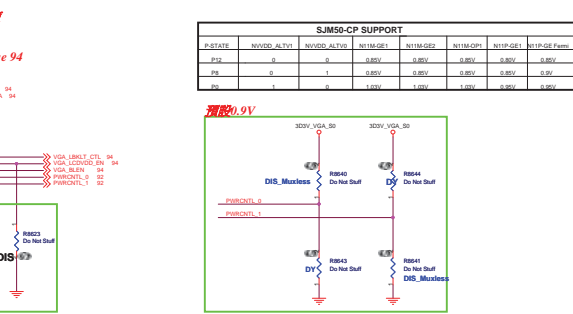
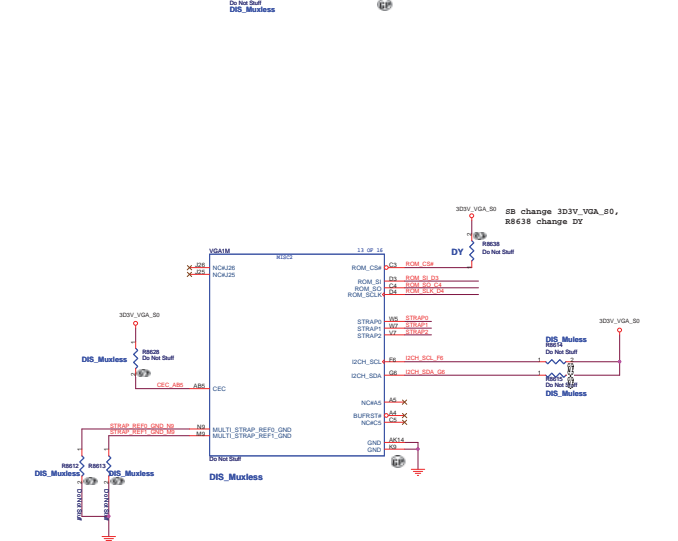
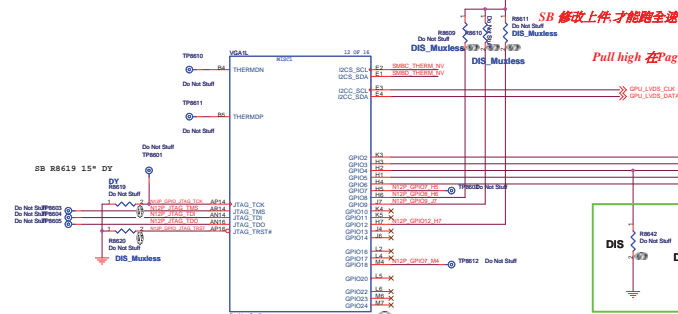
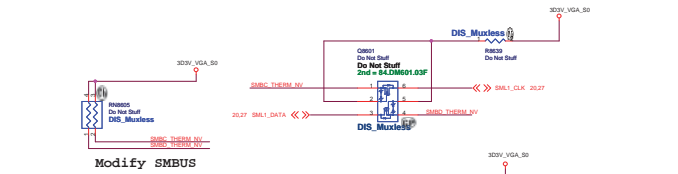
HR UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsien Ta Wu Rd., Hsichai, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
GPU Memory(2/5)			
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Date:	Thursday, December 02, 2010	Sheet	84 of 102

DC tolerance $\pm 75\text{mV}$
AC tolerance $\pm 50\text{mV} < 100\text{MHz}$



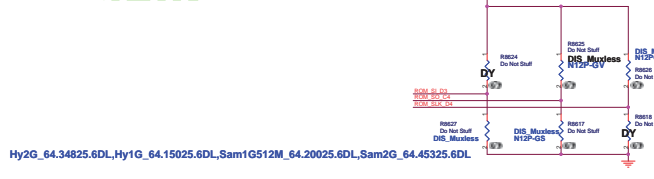
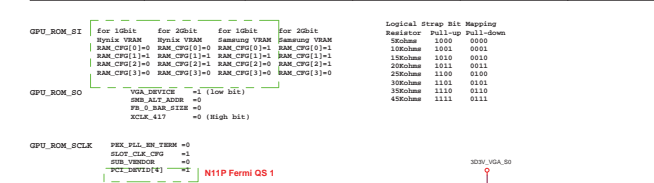


VGA Thermal sensor P2800

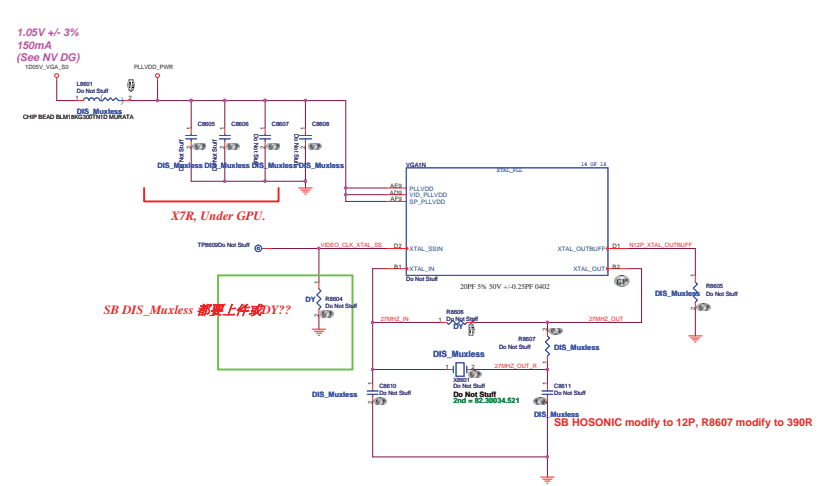


NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 0011 64*16*4 800MHZ	Samsung 2G 0110 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL



Hy2G_64.34825.6DL,Hy1G_64.15025.6DL,Sam1G512M_64.20025.6DL,Sam2G_64.45325.6DL

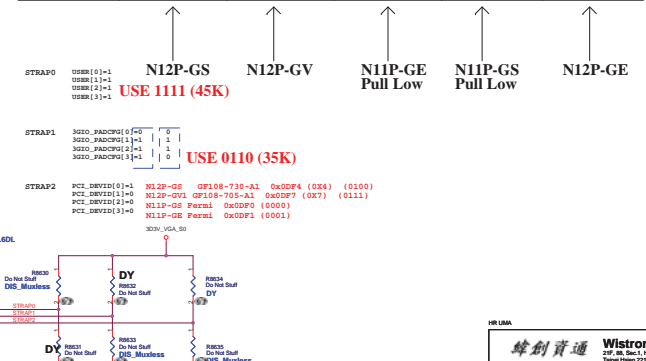


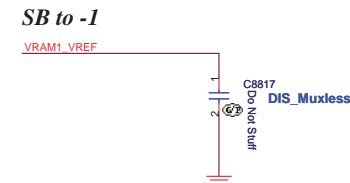
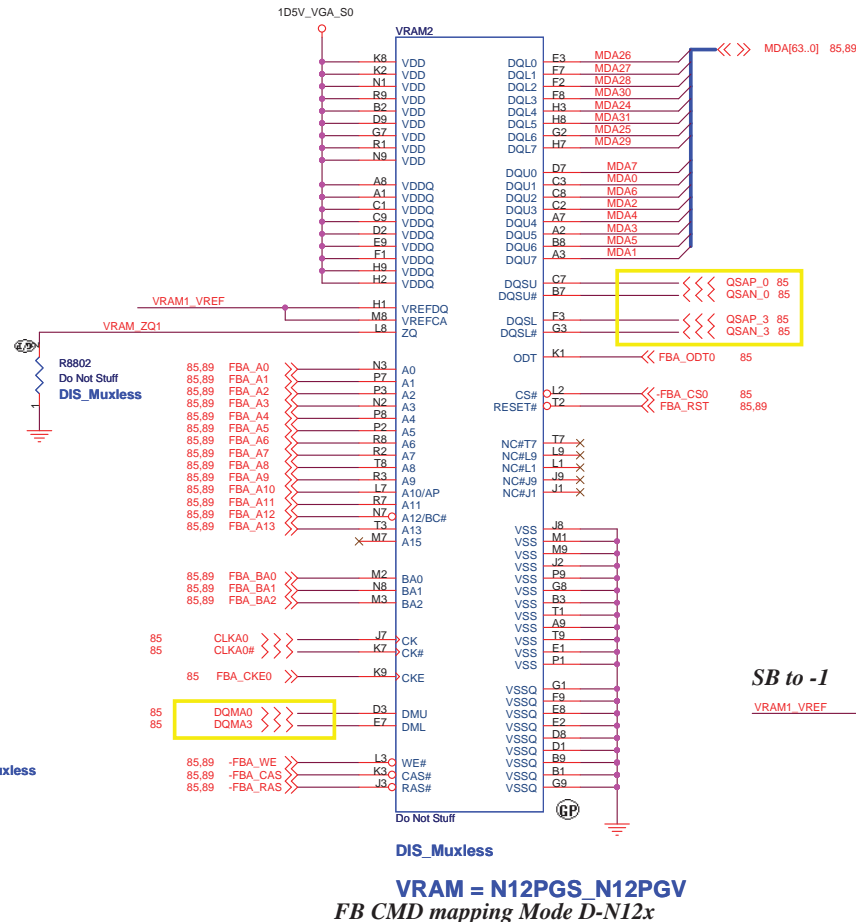
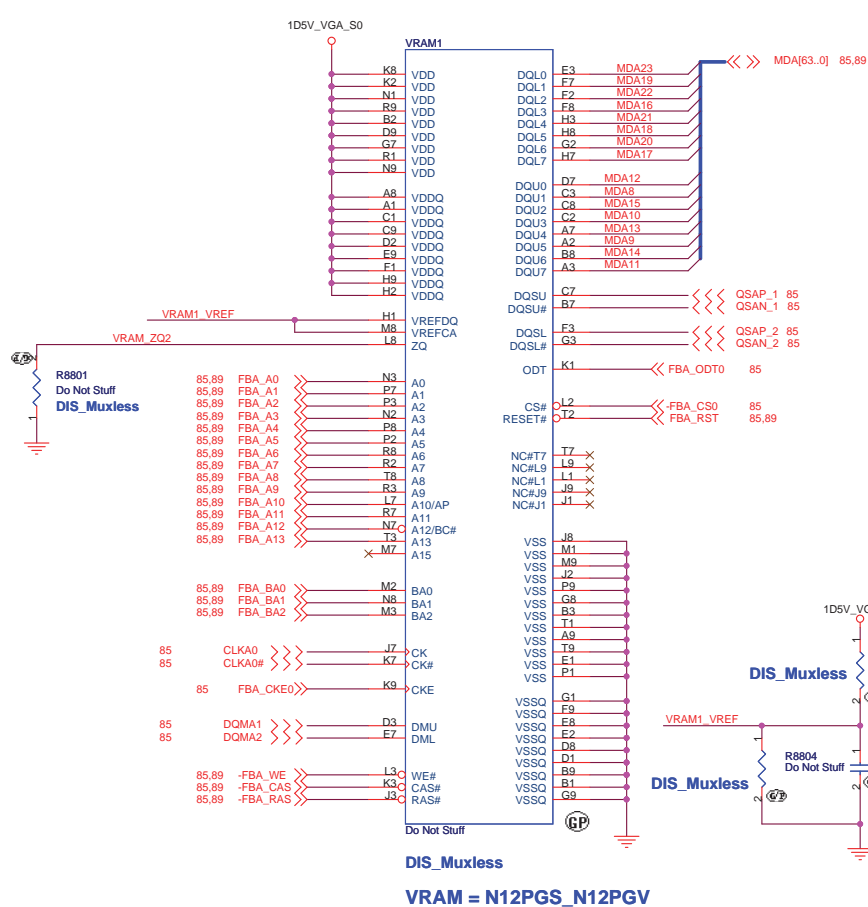
SB DIS_Muxless 都要上件或DY??

SB HOSONIC modify to 12P, R8607 modify to 390R

TABLE NVIDIA -1 modify N12P GV setting

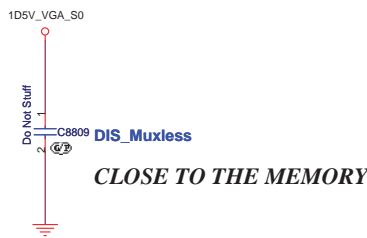
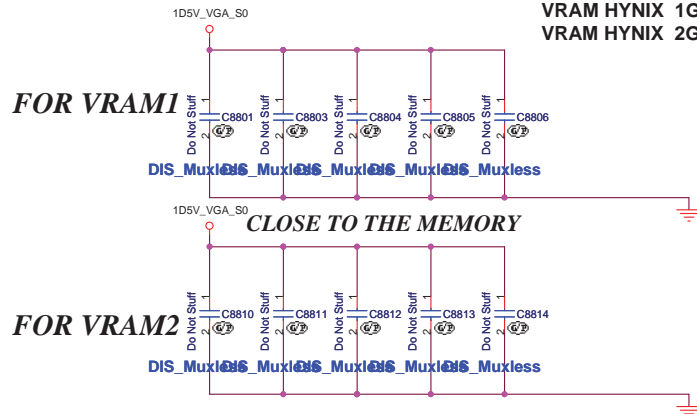
NVIDIA	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL





VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip



HR UMA

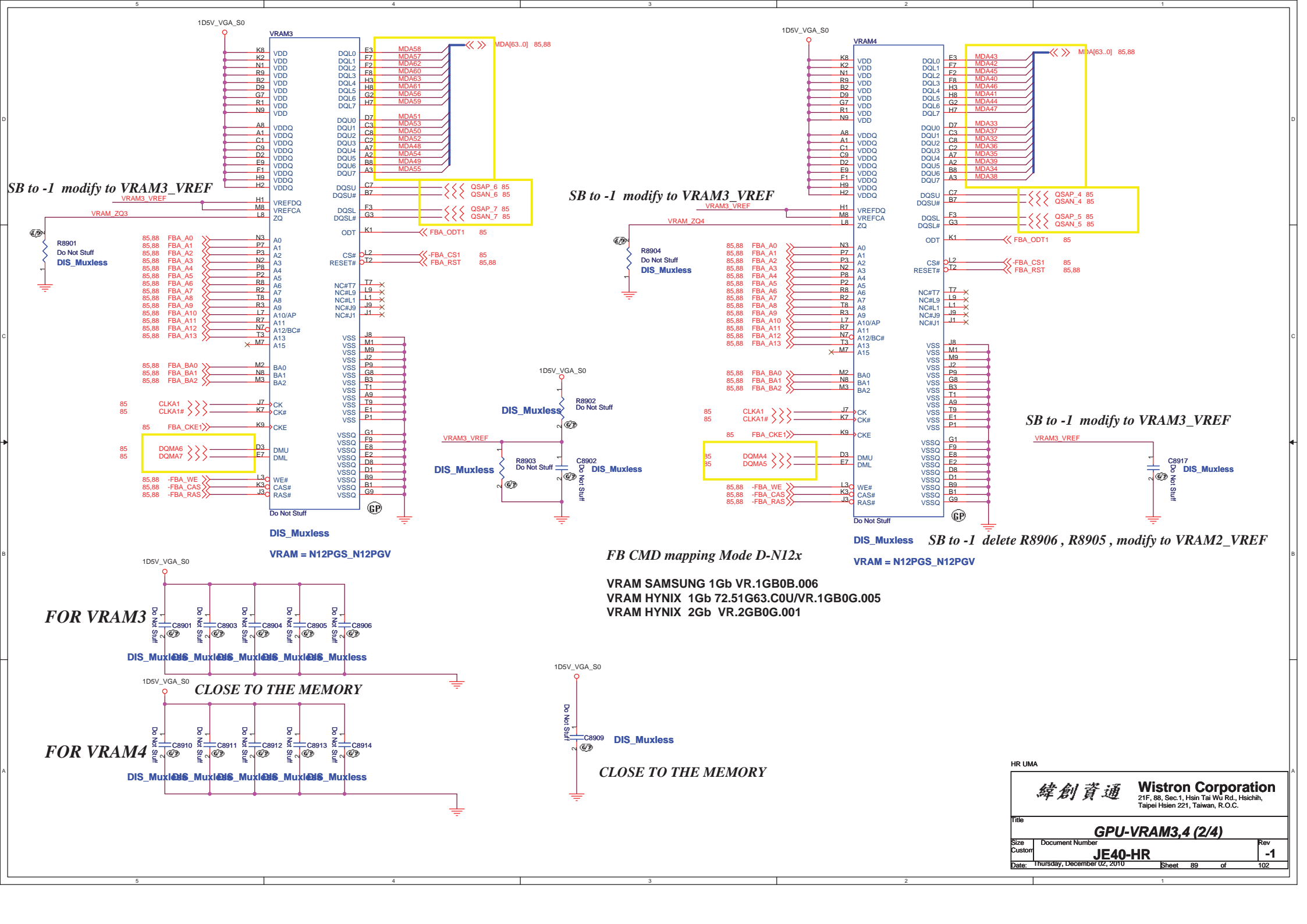
緯創資通 Wistron Corporation

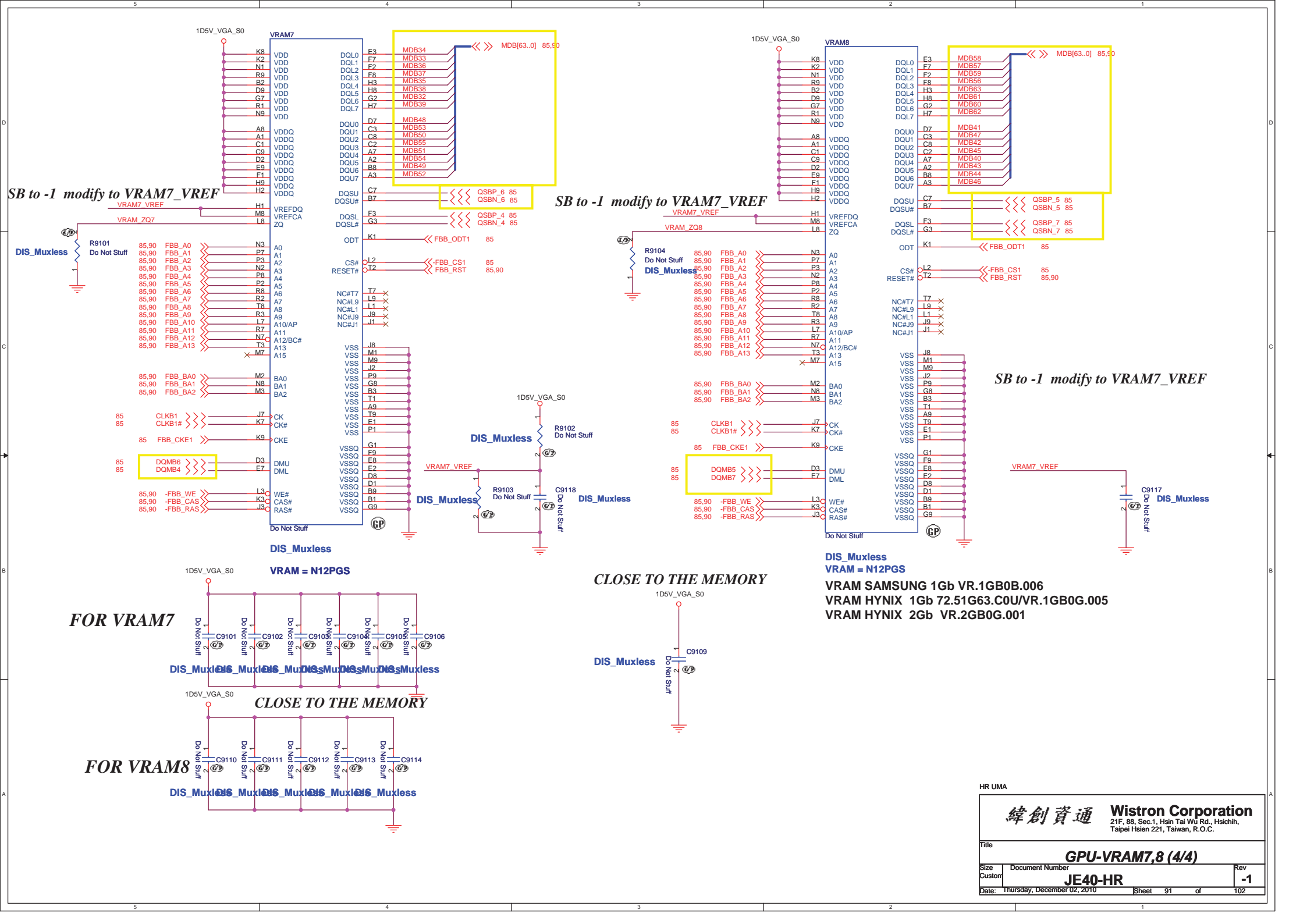
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **GPU-VRAM1,2 (1/4)**

Size Custom Document Number **JE40-HR** Rev **-1**

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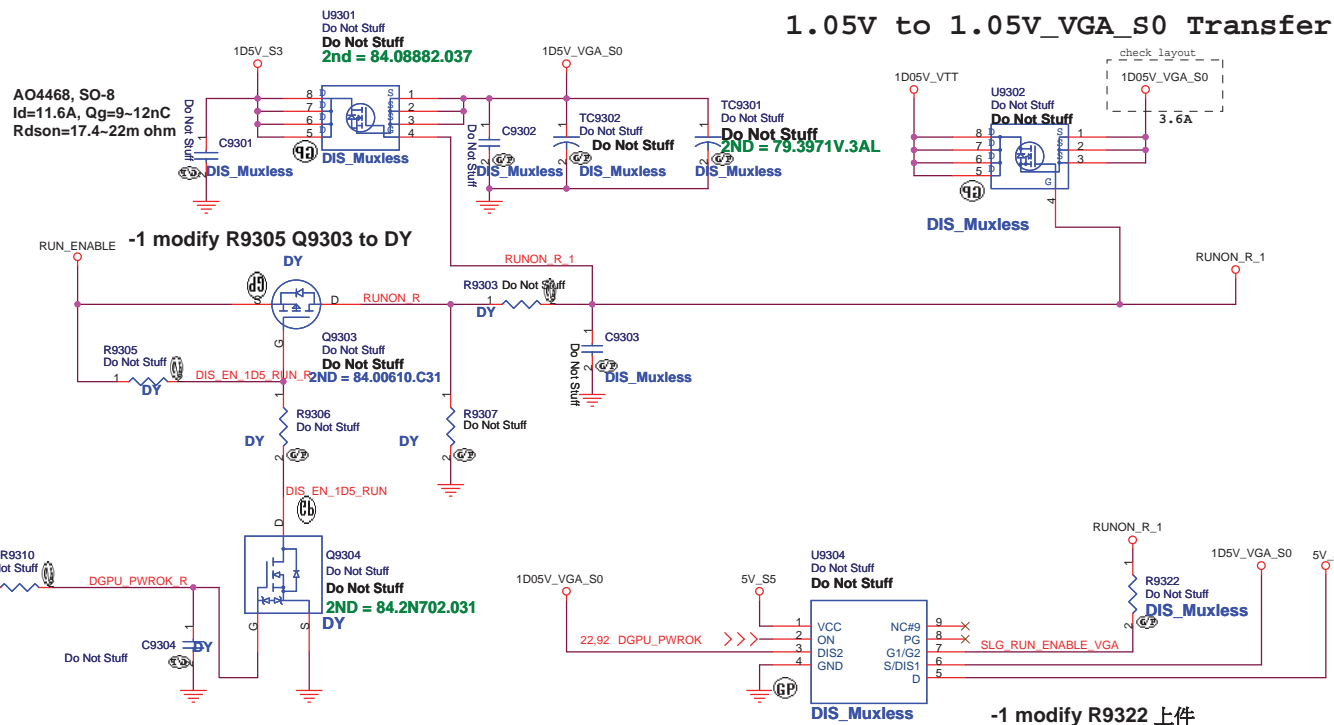




HR UMA		 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		RT8208B +VGA CORE	
Size	Document Number		Rev
Custom	JE40-HR		-1
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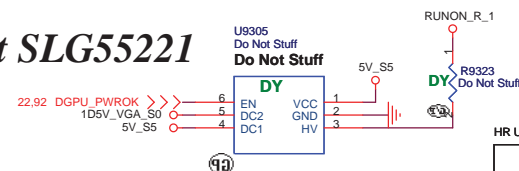
1D5V_VGA_S0

1.05V to 1.05V_VGA_S0 Transfer

[illegible]

1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

DISCRETE VGA POWER

Size	Custom
------	--------

Document Number

JE40-HR

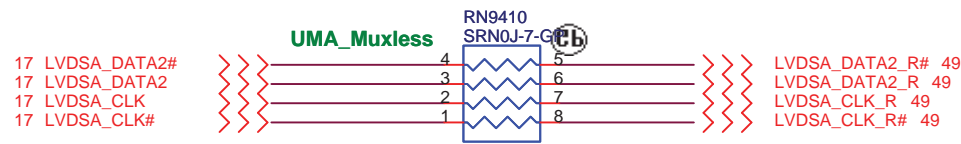
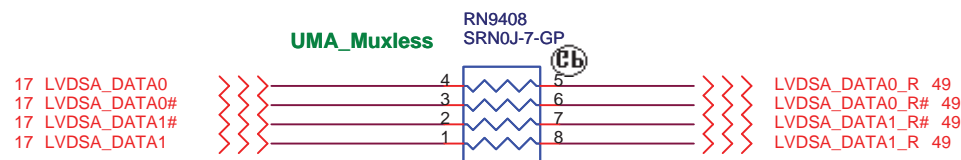
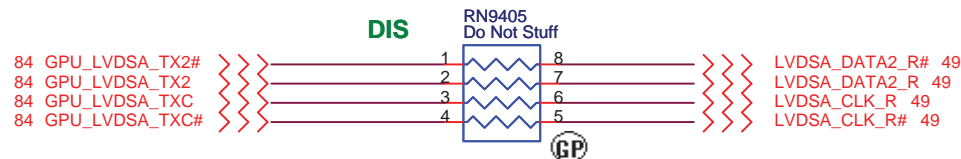
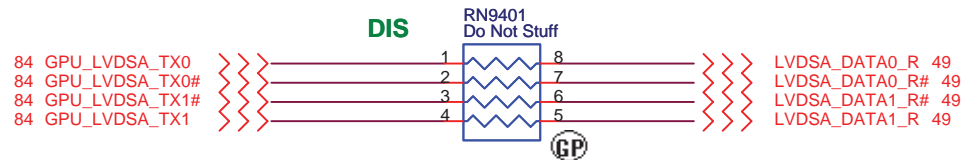
Date: Thursday, December 02, 2010

Sheet

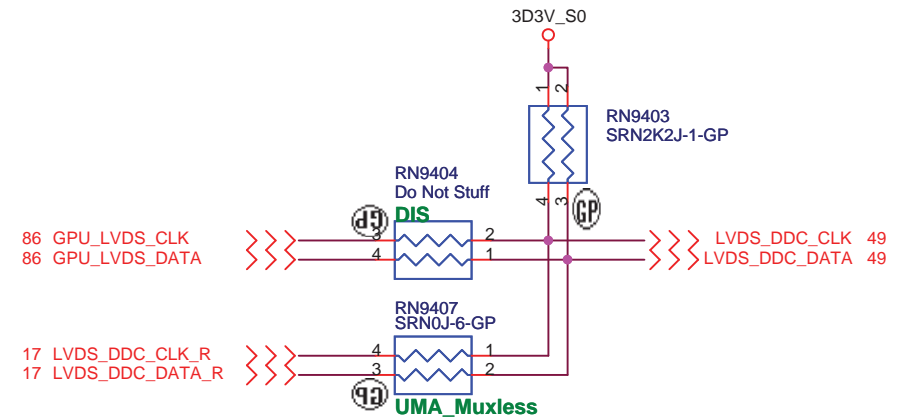
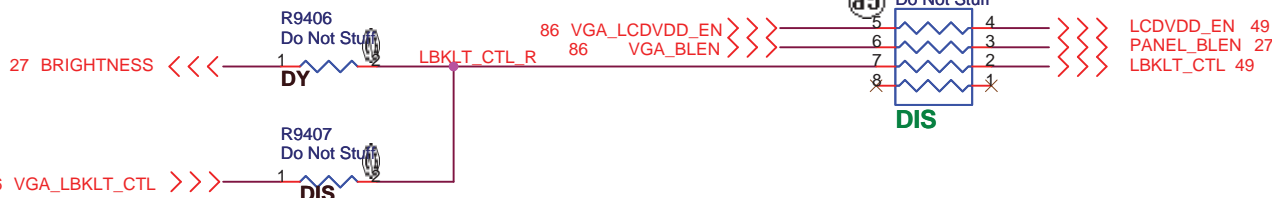
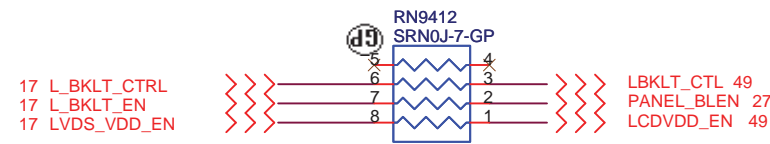
1

102

LVDS Channel A



Panel BL brightness/Power En/BL En



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Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size
A4

Document Number

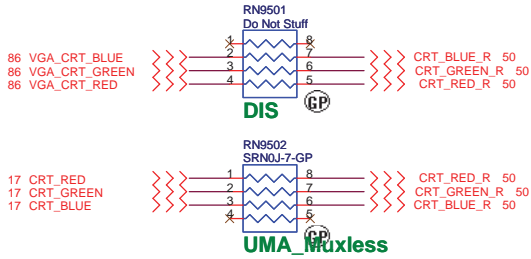
JE40-HR

Rev
-1

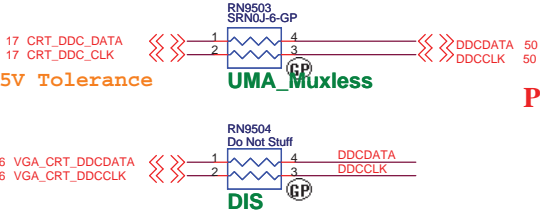
Date: Thursday, December 02, 2010

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Close to CRT Board CONN

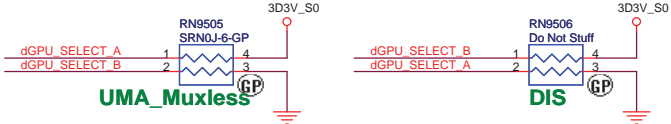


CRT DDCDATA & DDCCLK



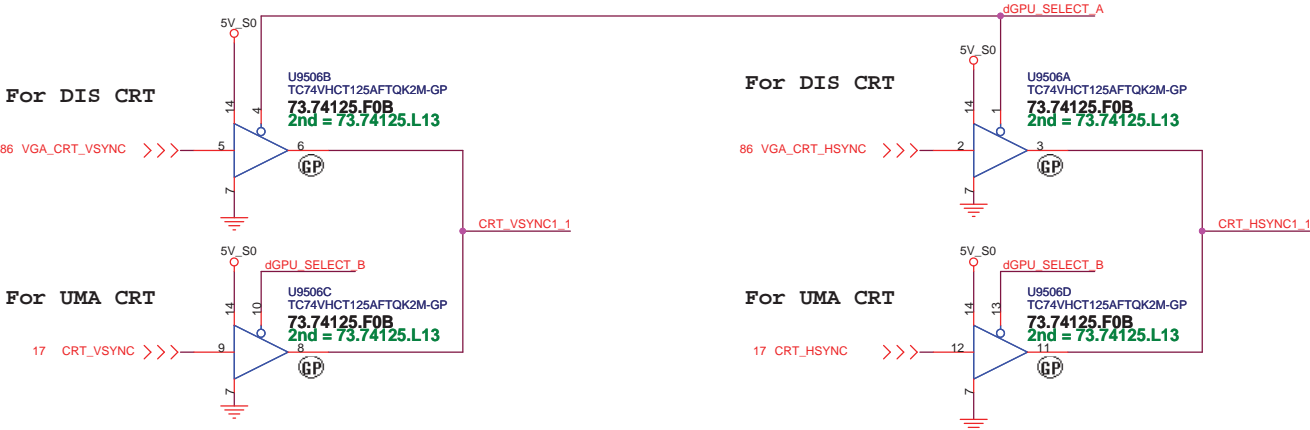
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA

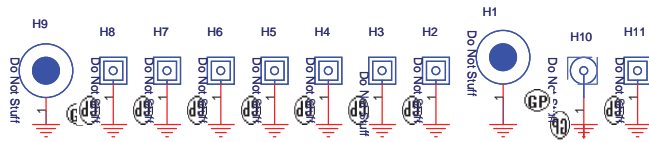


SB to -1 modify R9503,R9504 to 10 ohm



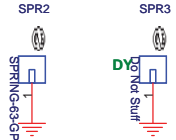
SSID = SDIO

HR LIMA		
<div>緯創資通Wistron Corporation</div> <div>21F, 8th, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title		
TOUCH PANEL		
Size	Document Number	Rev
A2	JE40-HR	-1
Date: Thursday, December 02, 2010		
Sheet 96 of 102		

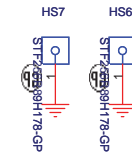
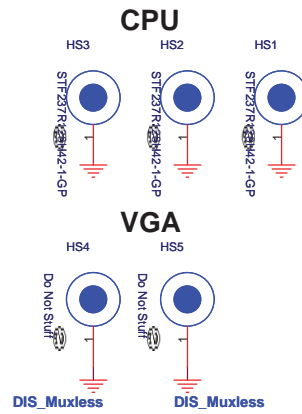
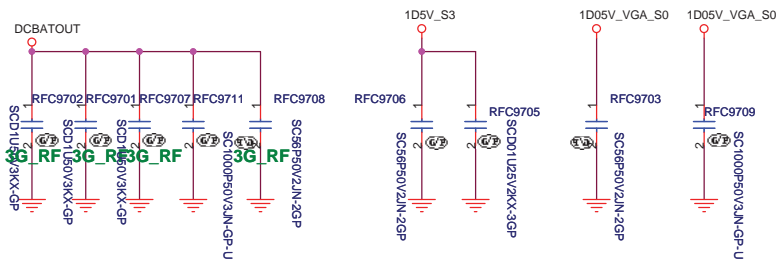
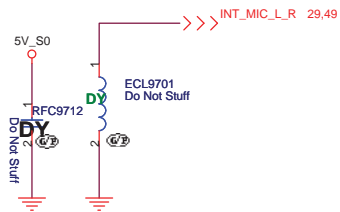
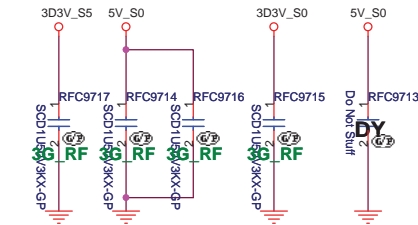


SB to -1 BOM add SPR2

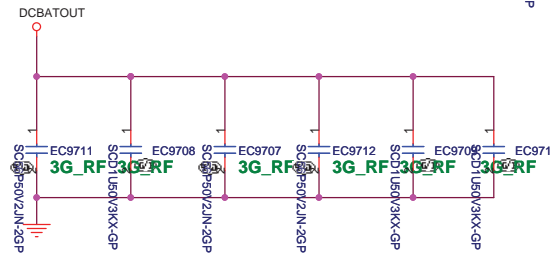
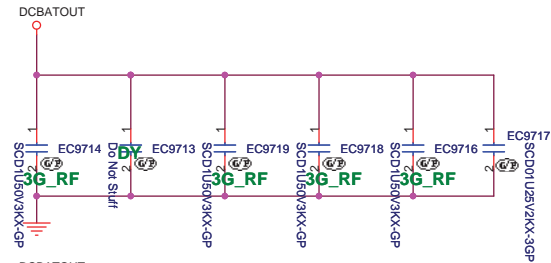
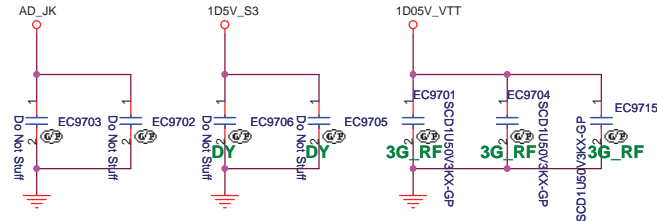
-2 delete SPR5



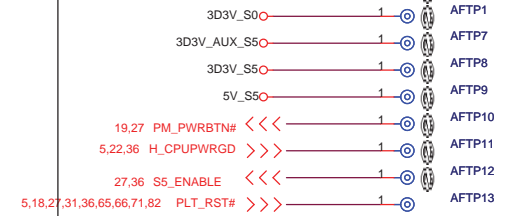
Change:34.40V16.001



3G Sku



Check test point



Test Point放在Dimm Door打開可量測處

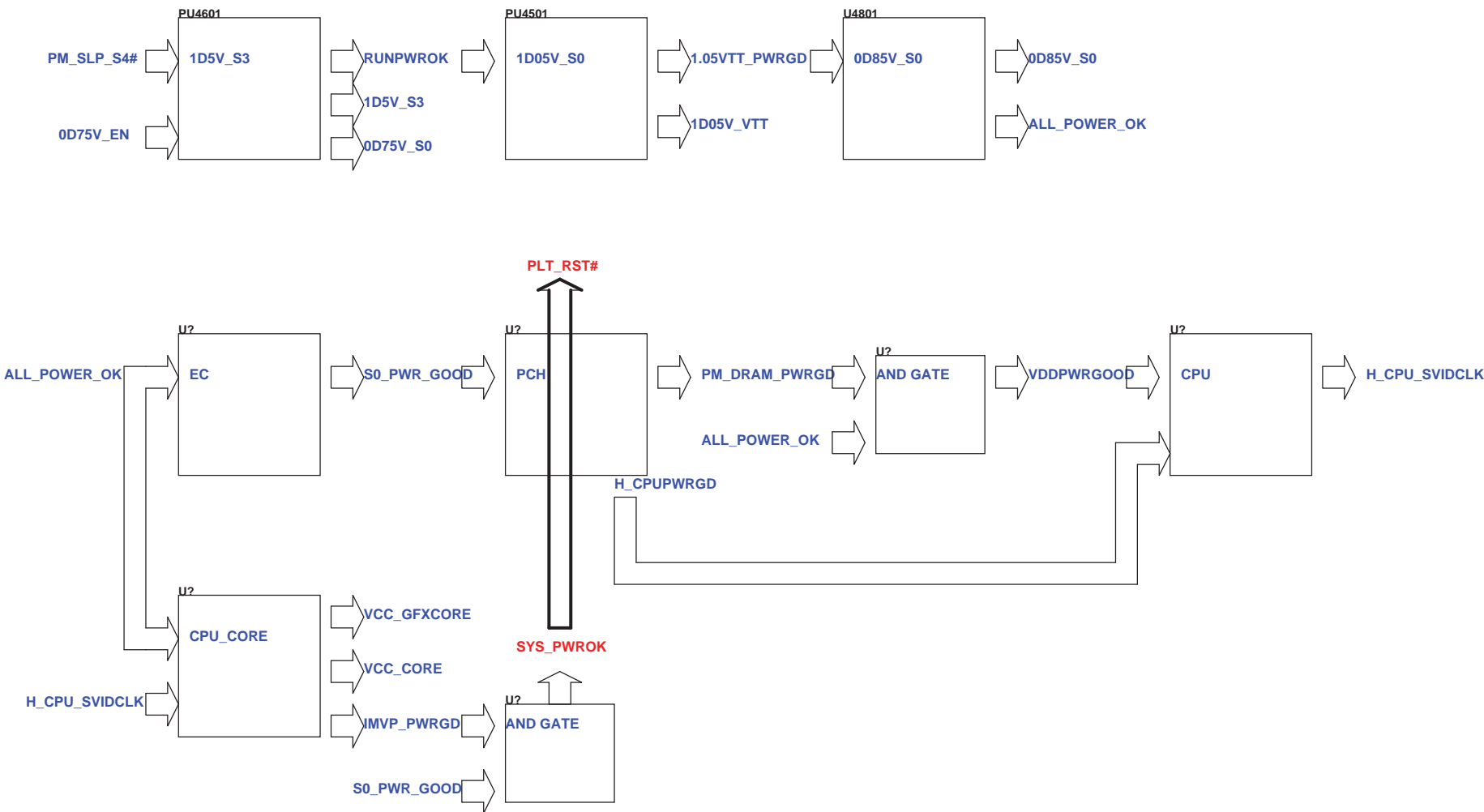
HR UMA

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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title UNUSED PARTS/EMI Capacitors		
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 97 of 102	

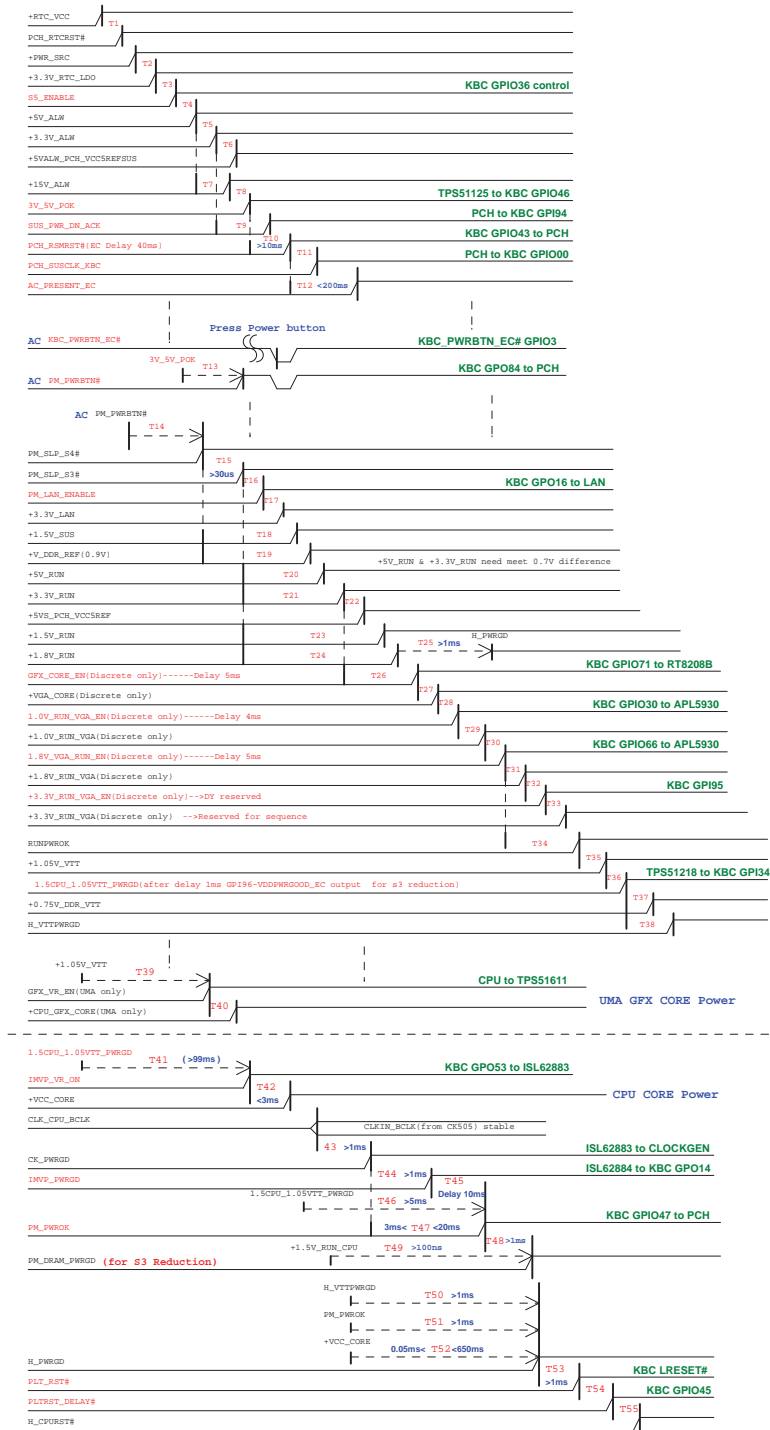
Power Sequence



Intel-Power Up Sequence

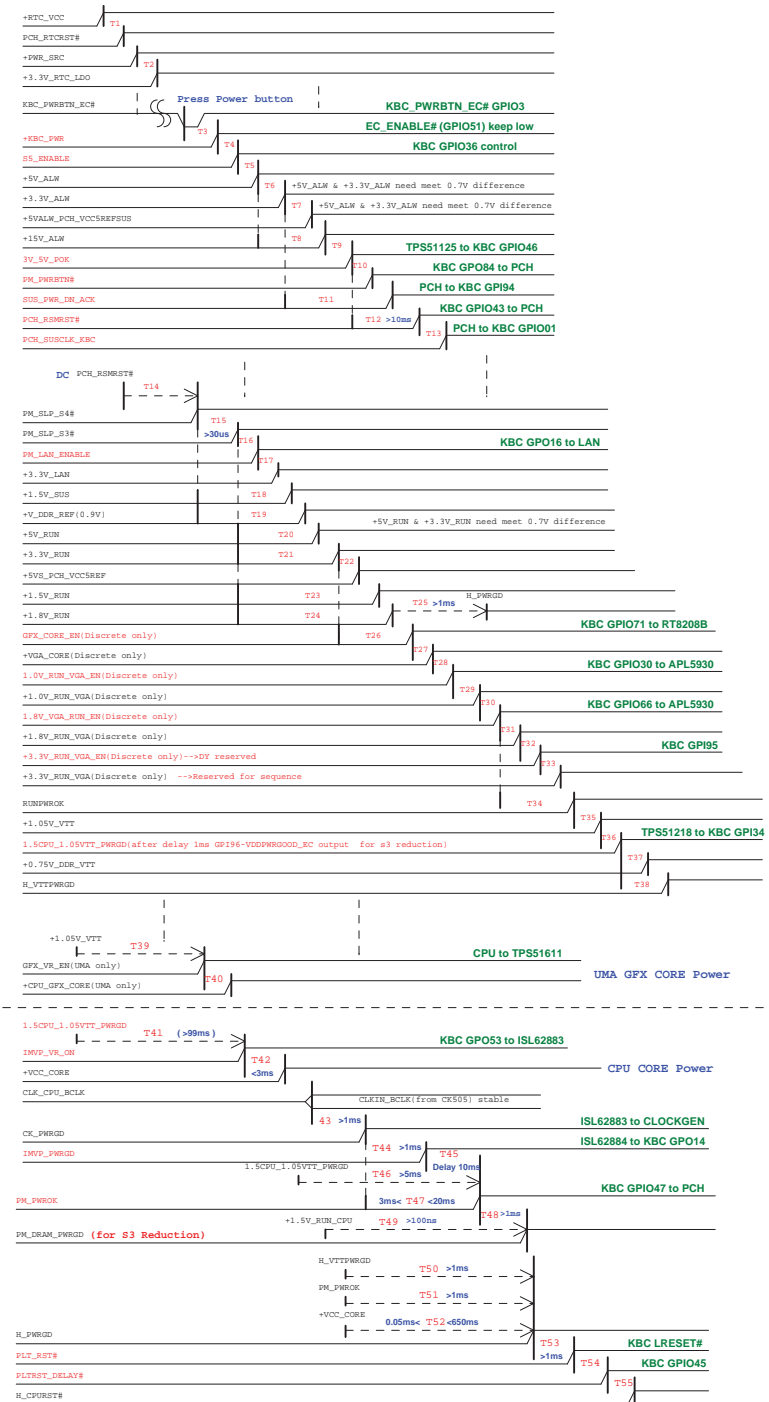
(AC mode)

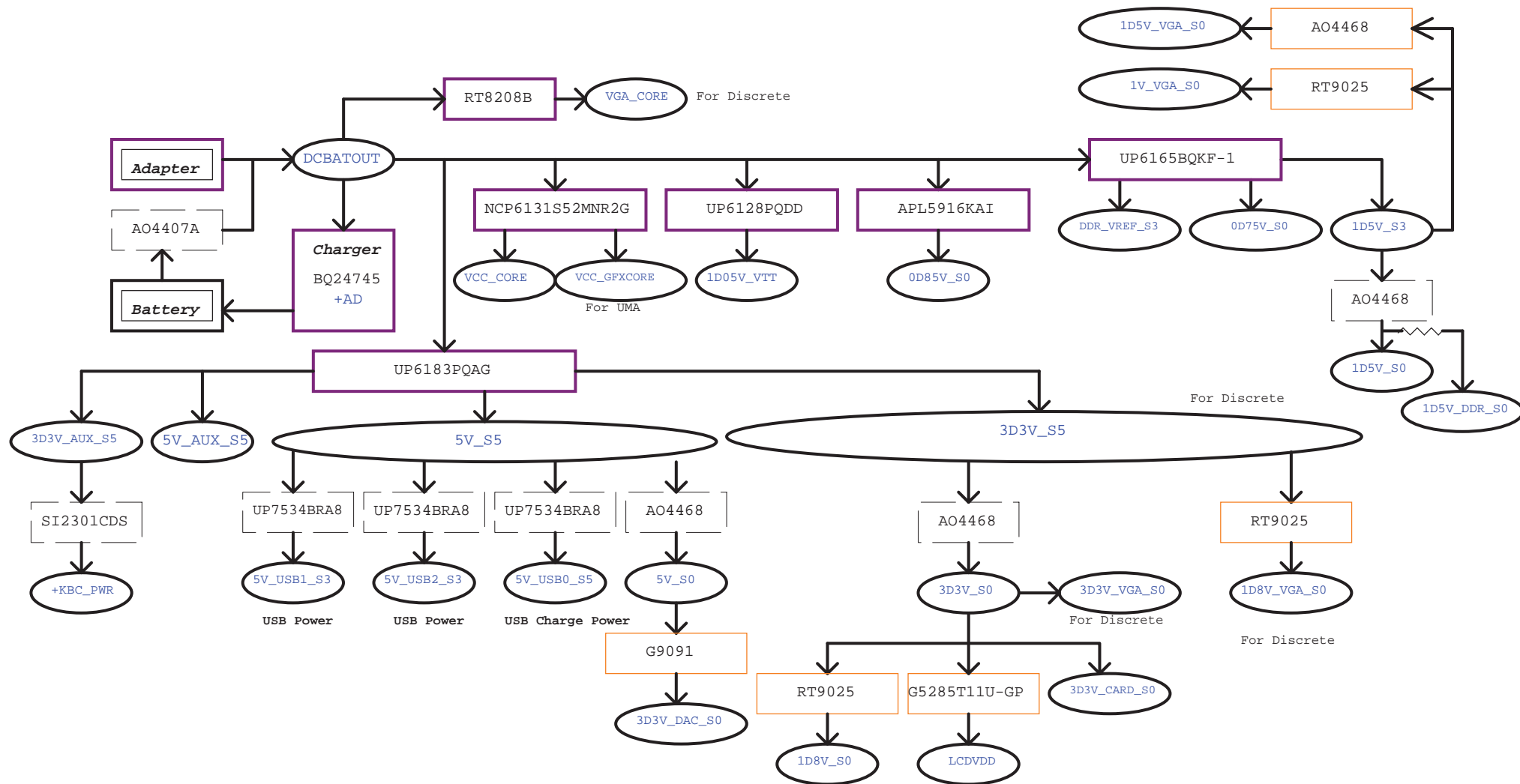
red word: KBC GPIO



(DC mode)

red word: KBC GPIO





Power Shape

Regulator

LDO

Switch

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

Size
A3

Document Number

JE40-HR

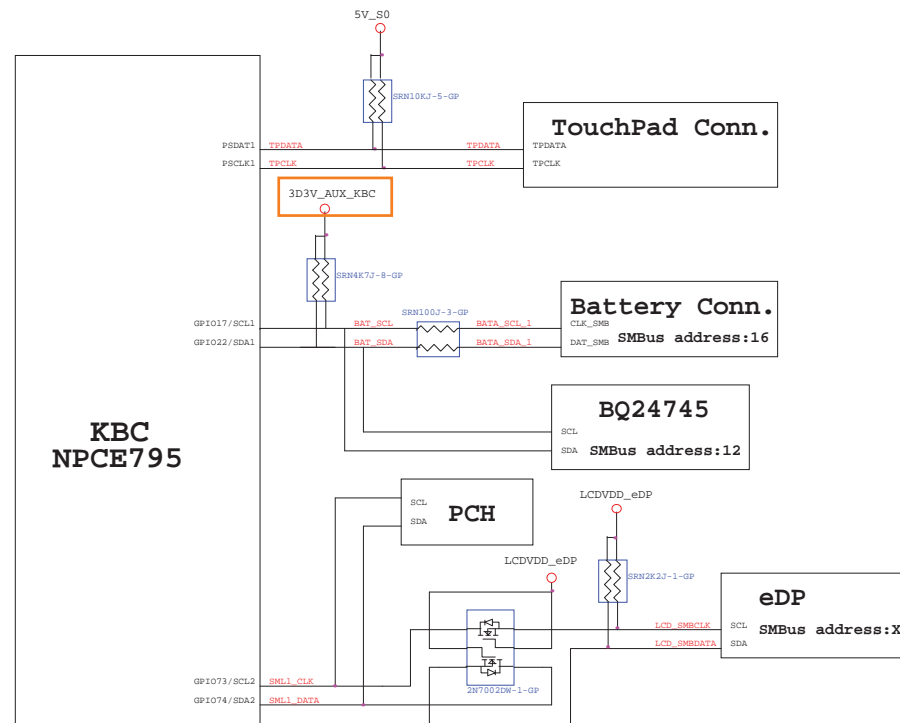
Rev

-1

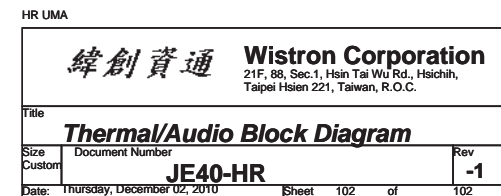
Date: Thursday, December 02, 2010

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KBC SMBus Block Diagram



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Codec
92HD79B1

SPKR_PORT_D_L-
SPKR_PORT_D_R+

SPEAKER

HP1_PORT_B_L
HP1_PORT_B_R

**HP
OUT**

HP0_PORT_A_L
HP0_PORT_A_R
VREFOUT_A_OR_F

**MIC
IN**

DMIC_CLK/GPIO1
DMIC0/GPIO2

**Digital
MIC**

PORTC_L
PORTC_R
VREFOUT_C

**Analog
MIC**